CA-IS2062 5kV$_{RMS}$ Isolated CAN Transceivers with Integrated DC-DC Converter

1 Features

- **Meets the ISO 11898-2 physical layer standards**
- **Integrated DC-DC converter for cable-side power**
- **Integrated protection increases robustness**
  - 5kV$_{RMS}$ withstand isolation voltage for 60s (galvanic isolation)
  - ±150kV/µs typical CMTI
  - ±58V fault-tolerant CANH and CANL
  - ±30V extended common-mode input range (CMR)
  - Transmitter dominant timeout prevents lockup, data rates down to 5.5 kbps
  - Thermal shutdown
  - Wide operating temperature range: -40°C to 125°C
- **Date rate is up to 1Mbps**
- **Operating from a single 5V supply on the logic side**
- **Low loop delay: 150ns (typical), 210ns (maximum)**
- **Ideal passive behavior when unpowered**
- **Wide-body SOIC16-WB(W) package**
- **Safety Regulatory Approvals**
  - VDE certification according to DIN EN IEC 60747-17(VDE 0884-17):2021-10
  - UL certification according to UL 1577
  - CQC certification according to GB4943.1-2022
  - TUV certification

2 Applications

- Industrial Controls
- Building Automation
- Security and Protection System
- Transportation
- Medical
- Telecom

3 General Description

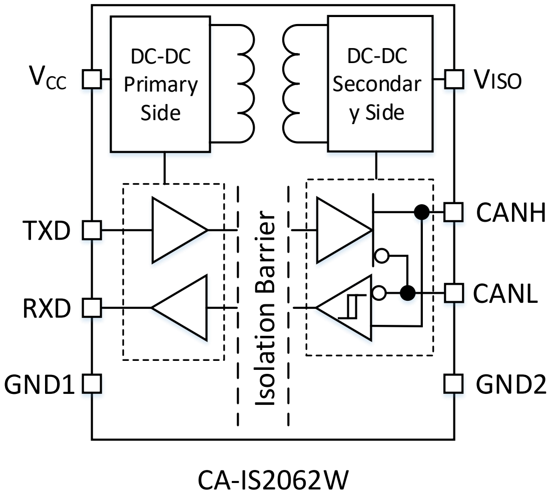
The CA-IS2062 is galvanically-isolated CAN transceivers with a built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained isolated designs. It has the logic input and output buffers separated by a silicon oxide (SiO2) insulation barrier that provides up to 5kV$_{RMS}$ (60s) of galvanic isolation. Isolation improves communication by breaking ground loops and reduces noise where there are large differences in ground potential between ports.

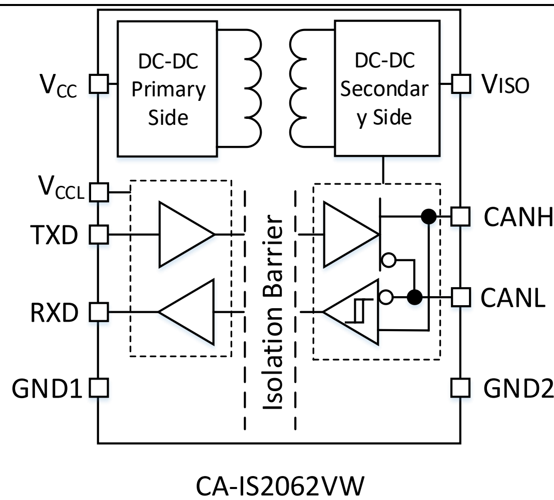
The CA-IS2062 operates from a single 5V supply on the logic side. An integrated DC-DC converter generates the 5V operating voltage for the cable-side. This device does not require any external components other than bypass capacitors to realize an isolated CAN port. The transceivers operate up to 1Mbps data rate and feature integrated protection for robust communication, including current limit, thermal shutdown, and the extended ±58V fault protection on the CAN bus for equipment where overvoltage protection is required. The dominant timeout detection prevents bus lockup caused by controller error or by a fault on the TXD input. These CAN receivers also incorporate an input common-mode range (CMR) of ±30V, exceeding the ISO 11898 specification of -2V to +7V.

The CA-IS2062 is available in wide-body 16 pin SOIC(W) package, operates over -40°C to +125°C temperature range.

Device information

Part Number	Package	Package size (nominal value)
CA-IS2062W CA-IS2062VW	SOIC16-WB(W)	10.30 mm × 7.50 mm





Simplified functional block diagram

4 Ordering Information

Table 4-1 Ordering Information

Part #	V_{CC} (V)	Data Rate (Mbps)	Galvanic Isolation (V_{RMS})	V_{CCL}	Package
CA-IS2062W	4.5~5.5	1	5000	No	SOIC16-WB(W)
CA-IS2062VW	4.5~5.5	1	5000	Yes	SOIC16-WB(W)

Contents

5 Revision History

Revision Number	Description	Revised Date	Page Changed
Version 1.00	NA	2022/07/12	NA
Version 1.01	Updated POD and UL certification information	2023/03/20	7
Version 1.02	Updated typical application circuit and PCB layout information	2023/05/20	19,20
Version 1.03	Update VDE, UL, TUV information	2023/10/23	6, 7
Version 1.04	Update CA-IS2062VW VCCL supply voltage range	2024/02/27	5
Version 1.05	Update VDE, UL, CQC, TUV information Update the test conditions of V_{IOSM}	2024/04/16	1, 6, 7
Version 1.06	Update the simplified functional block diagram Update the description of pin 7 of CA-IS2062VW Update the typical value of V_{CCL} Add I_{ISO} value and update its annotation Add I_{ISO} $V_{ISO\ (LINE)}$ and $V_{ISO\ (LOAD)}$, EFF Parameters Add notes to C_I, C_{ID}, CMTI parameters Update recommended PCB power supply routing	2024/05/14	2, 4, 5, 8, 9, 20
Version 1.07	Add TUV certification number of IEC62368-1 standard Update VDE information of V_{IMP} and V_{IOSM} Update recommended land pattern of the package	2024/12/17	7 6-7 18

6 Pin Configuration and Functions

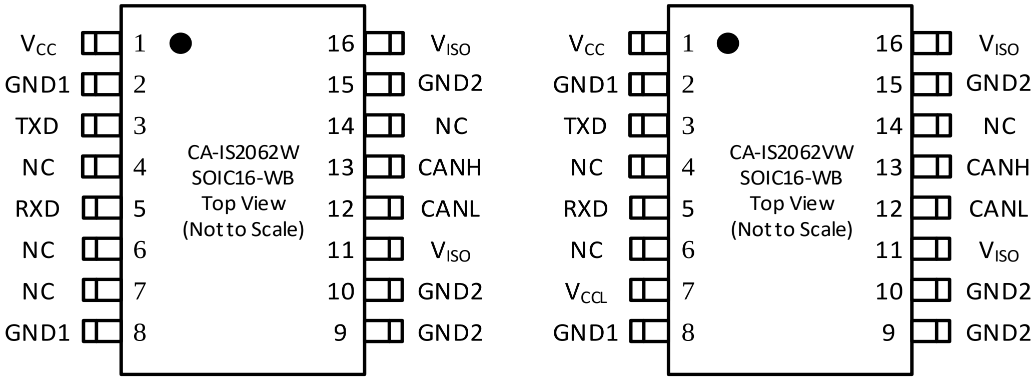


Figure 6-1 Pin Configuration

Table 6-1 CA-IS2062 Pin Configuration and Description

Pin name	Part number		Type	Description
	CA-IS2062W	CA-IS2062VW		
V_{CC}	1	1	Power supply	Power supply input for the logic side. Bypass V_{CC} to GND1 with 0.1µF//10µF capacitor as close to the device as possible.
GND1	2, 8	2, 8	Ground	Logic side ground.
TXD	3	3	Digital I/O	Transmitter data input. CANH and CANL are in the dominant state when TXD is low. CANH and CANL are in the recessive state when TXD is high.
NC	4, 6, 7, 14	4, 6, 14	-	No connection, do not connect these pins and leave them open.
V_{CCL}[1]	---	7	Power Supply	Logic-supply input. V_{CCL} is the logic supply voltage for logic-side input/output. Bypass to GND1 with a 1µF capacitor.
RXD	5	5	Digital I/O	Receiver output. RXD is high when the bus is in the recessive state. RXD is low when the bus is in the dominant state.
GND2	9, 10, 15	9, 10, 15	Ground	Bus side ground.
CANL	12	12	Differential I/O	Low-level CAN differential line.
CANH	13	13	Differential I/O	High-level CAN differential line.
V_{ISO}	11	11	Power supply input Pin	The power input pin for internal CAN, place a 1µF ceramic and keep the distance within 2mm.Connect this Pin to Pin16.
V_{ISO}	16	16	Power supply output Pin	Isolated power supply output, provide power for the cable-side. Bypass V_{ISO} to GND2 with 0.1µF//10µF capacitors as close to the device as possible.

7 Specifications

7.1 Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{CC} or V_{ISO}	Power supply voltage[2]	–0.5	6.0	V
TXD or RXD to GND1	Logic side voltage (RXD, TXD)	–0.5	V_{CC} + 0.5[3]	V
CANH or CANL to GND2	Bus side voltage (CANH and CANL)	–40	40	V
I_O	Receiver output current	–15	15	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	–65	150	°C

Notes:

1. The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground (GND1 or GND2) and are peak voltage values.
3. Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			Numerical value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±2000	

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3 Recommended Operating Conditions

Parameters			MIN	TYP	MAX	Unit
V_{CC}	Logic side power voltage		4.5	5	5.5	V
V_{CCL}	Logic side logic power voltage		2.375	2.5/3.3/5	5.5	V
V_I or V_{IC}	Voltage at bus pins (separately or common mode)		–12		12	V
V_{IH}	Input high voltage	Driver (TXD)	2		V_{CC} + 0.3	V
V_{IL}	Input low voltage	Driver (TXD)	–0.3		0.8	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–2			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			2.5	
T_A	Ambient temperature		–40	25	125	°C
T_J	Junction temperature		–40		150	°C
P_D	Total power dissipation	V_{CC} = 5.5V, T_A = 125°C, R_L = 60Ω, TXD input is 500 kHz, 50% duty cycle square wave			900	mW
$T_{J(shutdown)}$	Thermal shutdown temperature[1]			165		°C

Note:

1. Extended operation in thermal shutdown may affect device reliability.

7.4 Thermal Information

Heat meter		SOIC16-WB	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	°C/W

7.5 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-17:2021-10[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50 μs waveform per IEC 62368-1	9846	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test) , 1.2/50 μs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~3.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.6 Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17(VDE 0884-17):2021-10; EN IEC 60747-17:2020+AC:2021	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2022	Certified according to EN 61010-1 and EN 62368-1
Reinforced Isolation: V_{IORM}: 1414V_{pk} V_{IOTM}: 7070V_{pk} V_{IOSM}: 12800V_{pk}	Single protection 5000V_{RMS}	Reinforced isolation (Altitude ≤ 5000m)	EN 61010-1: 5000V_{RMS} EN 62368-1: 5000V_{RMS}
Certification number: 40057278	Certification number: E511334	Certification number: CQC23001406424	Client reference number: 2253313

7.7 Electrical Characteristics

over recommended operating conditions (unless otherwise noted). All typical values are at 25°C with V_{CC} = 5 V.

Parameters		Test conditions	MIN	TYP	MAX	Unit
Power supply current						
I_{CC} Logic side power supply current		V_I = 0 V , R_L = 60 Ω dominant timeout protection		90	120	mA
		V_I = V_{CC}		10	20	
Isolated Power Supply						
V_{ISO} Output voltage		I_{ISO} = 0mA	4.75	5	5.25	V
I_{ISO}[1] Maximum load current[1]		R_L = NC [2]	130			mA
		R_L = 60Ω	90			
		R_L = 45Ω	80			
$V_{ISO(LINE)}$ DC line regulation		I_{ISO} = 50mA, V_{CC} = 4.5V to 5.5V		2	3	mV/V
$V_{ISO(LOAD)}$ DC load regulation		I_{ISO} = 0 to 130mA		1%	1.5%	
EFF Efficiency @ maximum load current		I_{ISO} = 130mA, C_{LOAD} = 0.1μF || 10μF	45%	53%		
Driver						
$V_{O(D)}$ Bus output voltage (dominant)	CANH	V_I = 0 V, R_L = 60 Ω; see *Figure 8-1* and *Figure 8-2.*	2.9	3.4	4.5	V
	CANL		0.5		2	
$V_{O(R)}$ Bus output voltage (recessive)		V_I = 2 V, R_L = 60 Ω; see *Figure 8-1* and *Figure 8-2.*	2	2.5	3	V
$V_{OD(D)}$ Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω; see *Figure 8-1, Figure 8-2* and *Figure 8-3.*	1.5		3	V
		V_I = 0 V, R_L = 45 Ω; see *Figure 8-1, Figure 8-2* and *Figure 8-3.*	1.3		3	V
$V_{OD(R)}$ Differential output voltage (recessive)		V_I = 3 V, R_L = 60 Ω; see *Figure 8-1* and *Figure 8-2.*	–80		80	mV
		V_I = 3 V, no-load.	–0.05		0.05	V
$V_{OC(D)}$ Common mode output voltage (dominant)		See Figure 8-7	2	2.5	3	V
$V_{OC(pp)}$ Peak to peak common mode output voltage				60		mV
I_{IH} High-level input current, TXD input		V_I = 2 V			20	μA
I_{IL} Low-level input current, TXD input		V_I = 0.8 V	–20			μA
$I_{OS(SS)}$ Short-circuit steady-state output current		V_{CANH} = –30 V, CANL open; see *Figure 8-10.*	–105	–36		mA
		V_{CANH} = 30 V, CANL open; see *Figure 8-10.*		0.6	2	
		V_{CANL} = –30 V, CANH open; see *Figure 8-10.*	–2	–0.6		
		V_{CANL} = 30 V, CANH open; see *Figure 8-10.*		42	105	
Receiver						
V_{IT+} Positive-going bus input threshold voltage				0.8	0.9	V
V_{IT-} Negative-going bus input threshold voltage			0.5	0.65		V
V_{HYS} Hysteresis voltage			50	125		mV
V_{OH} High-level output voltage		I_{OH} = –4 mA; see *Figure 8-6.*	V_{CC} – 0.8	4.8		V
		I_{OH} = –20 μA; see *Figure 8-6.*	V_{CC} – 0.1	5		
V_{OL} High-level output voltage		I_{OL} = 4 mA; see *Figure 8-6.*		0.2	0.4	V
		I_{OL} = 20 μA; see *Figure 8-6.*		0	0.1	
C_I[3] CANH or CANL input capacitance to ground		V_{TXD} = 3V, V_I = 0.4xsin(2πft)+2.5 V, f = 1MHz		24		pF
C_{ID}[3] Differential input capacitance		V_{TXD} = 3V, V_I = 0.4xsin(2πft), f = 1MHz		12		pF
R_{IN} CANH and CANL input capacitance		V_{TXD} = 3V	15		40	kΩ
R_{ID} Differential input resistance		V_{TXD} = 3V	30		80	kΩ
$R_{I(m)}$ Input resistance matching (1 – [$R_{IN(CANH)}$ / $R_{IN(CANL)}$]) x 100%		V_{CANH} = V_{CANL}	–2%	0%	2%	

CMTI[3] Common mode transient immunity	V_I = 0 V or V_{CC}; see *Figure 8-11.*	100	150		kV/µs

Notes:
1. The available output current from V_{ISO} will be reduced when T_A > 85̊C, the maximum output current should be appropriately reduced.
2. R_L = NC means no-load connection between CANH and CANL.
3. The test data is based on bench test and design simulation.

7.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted). All typical values are at 25°C with V_{CC} = 5 V.

Parameters		Test conditions	MIN	TYP	MAX	Unit
Device						
t_{loop1}	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	see *Figure 8-8.*	110	150	210	ns
t_{loop2}	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	see *Figure 8-8.*	110	150	210	ns
Driver						
t_{PLH}	TXD propagation delay (recessive to dominant)	see *Figure 8-4.*	35	75	130	ns
t_{PHL}	TXD propagation delay (dominant to recessive)	see *Figure 8-4.*	35	55	100	ns
t_r	Differential driver output rise time	see *Figure 8-4.*		55	100	ns
t_f	Differential driver output fall time	see *Figure 8-4.*		60	105	ns
t_{TXD_DTO}[1]	TXD dominant timeout	C_L = 100 pF; see *Figure 8-9.*	2	5	8	ms
Receiver						
t_{PLH}	RXD propagation delay (recessive to dominant)	see *Figure 8-6.*		85	140	ns
t_{PHL}	RXD Propagation delay (dominant to recessive)	see *Figure 8-6.*		60	140	ns
t_r	RXD Output signal rise time	see *Figure 8-6.*		2.5	6	ns
t_f	RXD Output signal fall time	see *Figure 8-6.*		2.5	6	ns

Note:
1. The TXD dominant time out (t_{TXD_DTO}) disables the driver of the transceiver once the TXD has been dominant longer than (t_{TXD_DTO}) which releases the bus lines to recessive preventing a local failure from locking the bus dominant.

8 Parameter Measurement Information

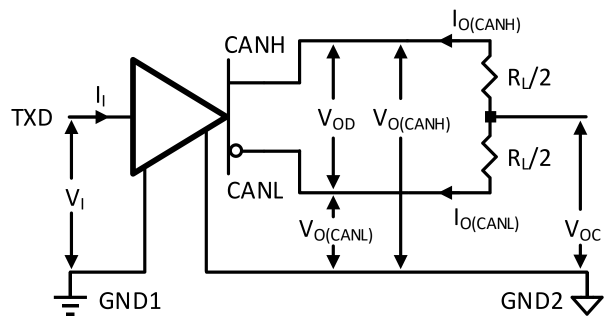


Figure. 8-1 Driver Voltage and Current Definition

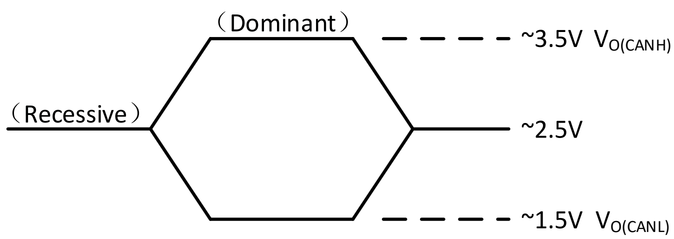


Figure. 8-2 Bus Logic State Voltage Definition

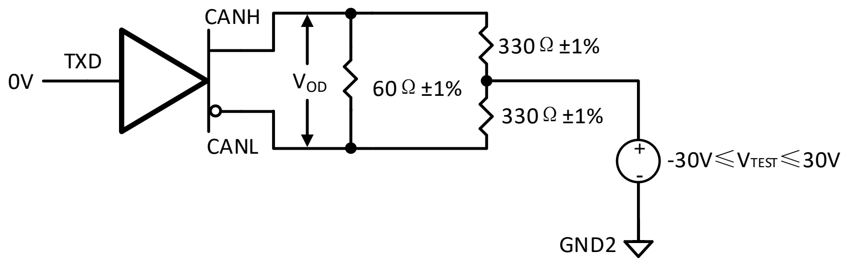
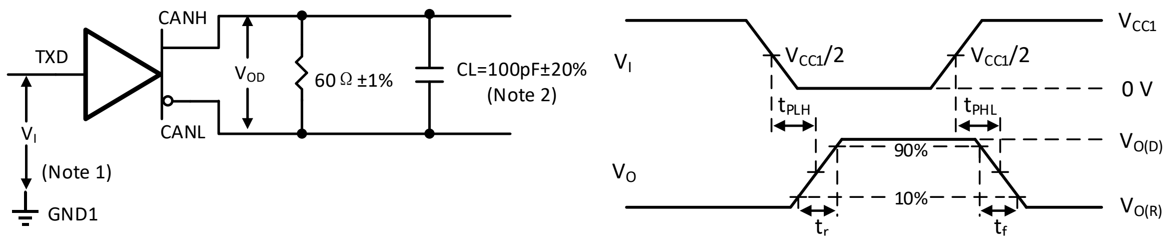


Figure. 8-3 Driver V_{OD} with Common Mode Loading Test Circuit



Notes:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125 kHz, 50% duty cycle; rise time $t_r \leq 6$ ns, fall time $t_f \leq 6$ ns; Z_O = 50 Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure. 8-4 Transmitter Test Circuit and Timing Diagram

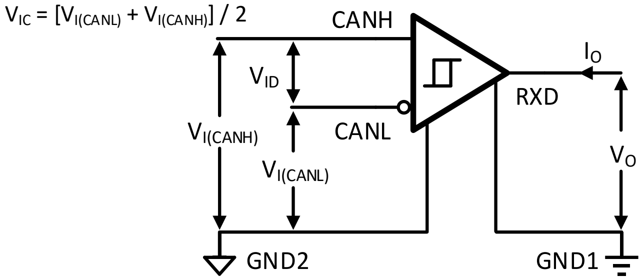
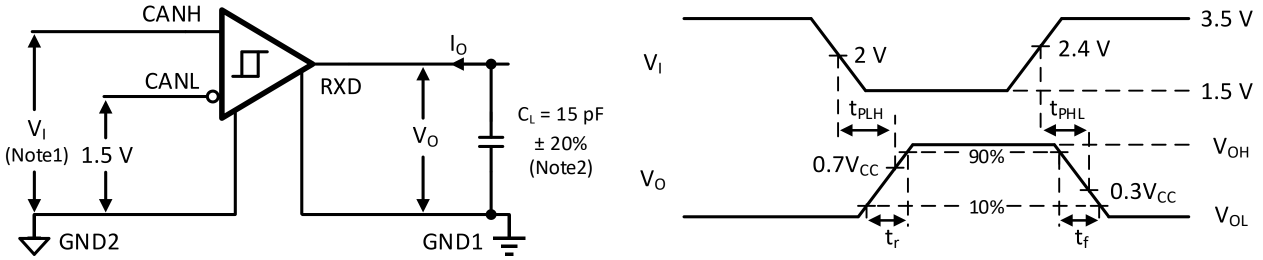


Figure. 8-5 Receiver Voltage and Current Definition



Notes:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125 kHz, 50% duty cycle; rise time t_r≤6 ns, fall time t_f≤6 ns; Z_O = 50 Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure. 8-6 Receiver Test Circuit and Timing Diagram

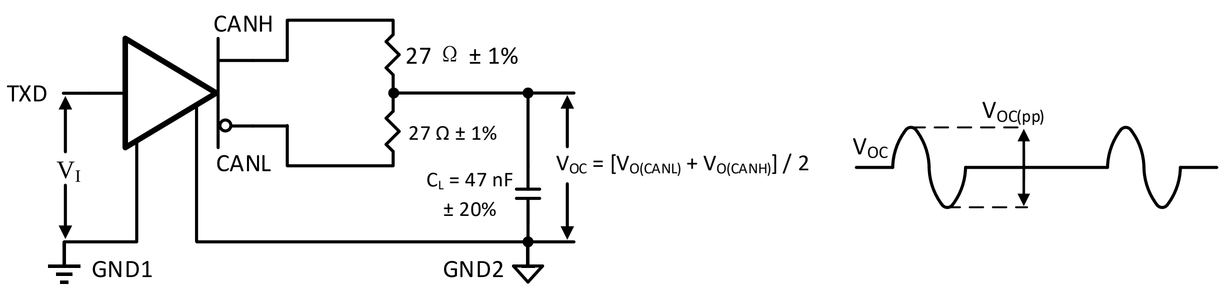


Figure. 8-7 Peak-to-Peak Output Voltage Test Circuit and Waveform

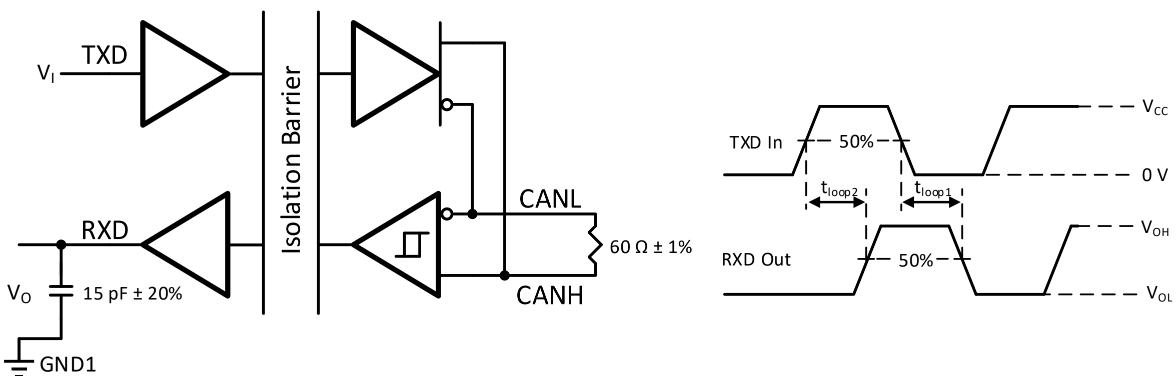
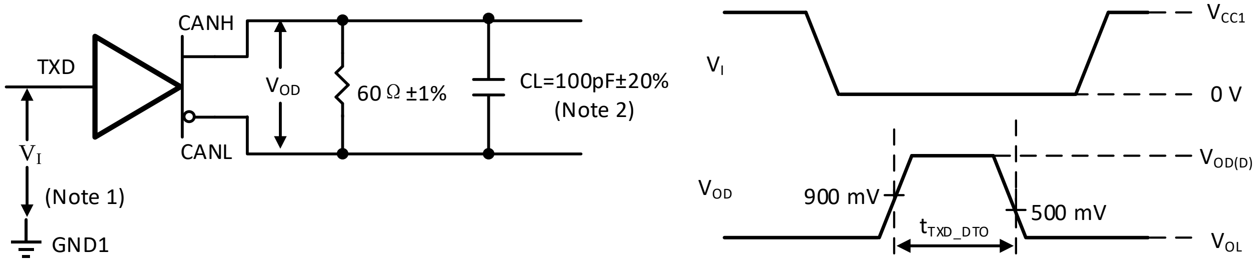


Figure. 8-8 TXD to RXD Loop Delay



Notes:

1. The input pulse is supplied by a generator with characteristics: PRR ≤ 125 kHz, 50% duty cycle; rise time t_r≤6 ns, fall time t_f≤6 ns; Z_O = 50 Ω.
2. Load capacitance C_L includes external circuit (instrumentation and fixture etc.) capacitance.

Figure. 8-9 Transmitting Dominant Timeout Timing Diagram

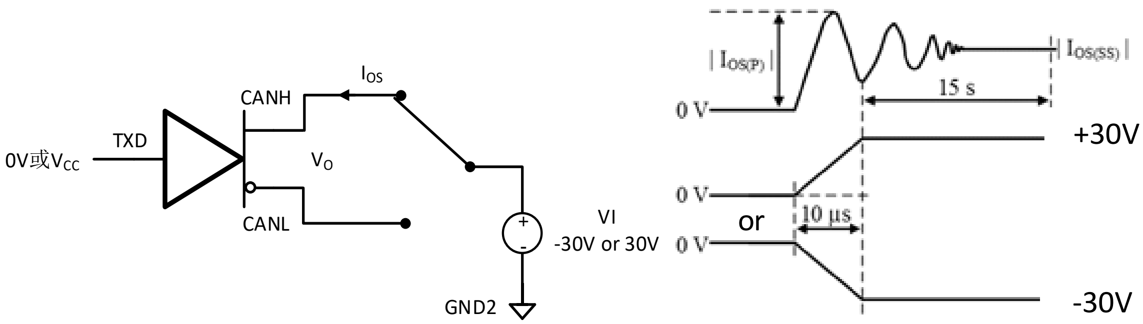


Figure. 8-10 Driver Short Circuit Current Test Circuit and Measurement

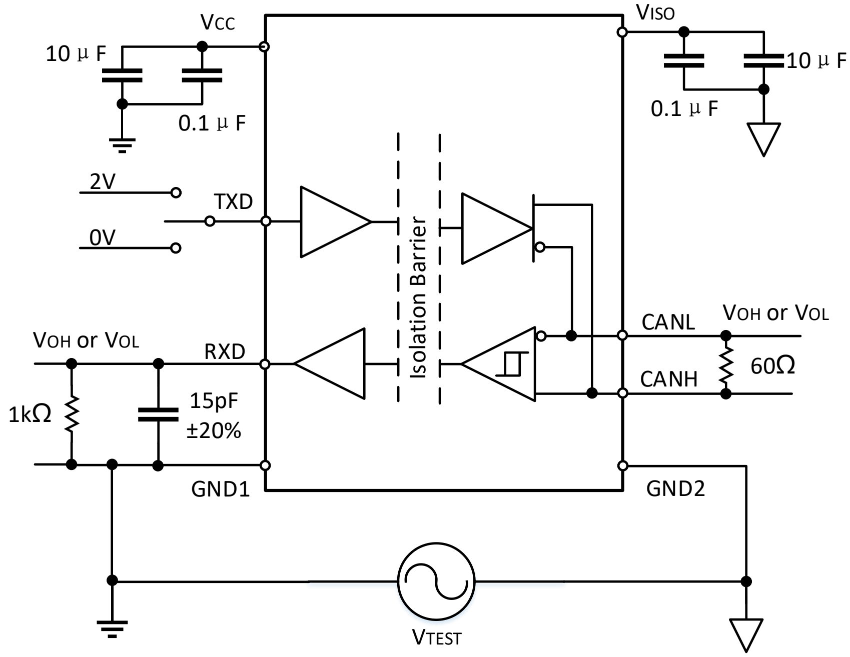


Figure. 8-11 Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The CA-IS2062 isolated CAN transceiver provides up to 3750V_{RMS} (60s) of galvanic isolation between the CAN cable-side of the transceiver and the logic-side. This integrated transceiver is suitable for applications that have limited board space and require more integration. Only external bypass capacitors are needed to fully realize an isolated CAN port. The device features up to 150 kV/µs common mode transient immunity, allow up to 1Mbps communication across an isolation barrier. Robust isolation coupled with high standoff voltage and increased speeds enables efficient communication in noisy environments, making it ideal for communication with the microcontroller in a wide range of applications such as industrial control, building automation, telecom rectifiers, HVACs etc. industrial applications. The supply voltage range for the logic side is 4.5V to 5.5V (V_{CC}); Power isolation is achieved with an integrated DC-DC convertor to generate a regulated 5V supply for the cable-side. The receiver input common-mode range is ±30V, exceeding the ISO 11898 specification of -2V to +7V, and the fault tolerant is up to ±58V. Dominant timeout prevents the bus from being blocked by a hung-up microcontroller, and the outputs CANH and CANL are short-circuit current-limited, protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

9.2 CAN Bus Status

The CAN bus has two states: dominant and recessive. In the dominant state (a zero bit, used to determine message priority), CANH-CANL are defined to be logic ‘0’ when the voltage across them is between +1.5V and +3V (higher than 0.9V). In the recessive state (a 1-bit and the state of the idle bus), the driver is defined to be logic ‘1’ when differential voltage is between -80mV and +80mV, or when it is near zero(lower than 0.5V), see *Figure 8-2*.

9.3 Receiver

The receiver reads the differential input from the bus line (CANH and CANL) and transfers this data as a single-ended output RXD to the CAN controller. The internal comparator senses the difference voltage V_{DIFF} = (V_{CANH}-V_{CANL}), with respect to an internal threshold of 0.7V. If V_{DIFF} > 0.9V, a logic-low is present on RXD; If V_{DIFF} < 0.5V, a logic-high is present. The CANH and CANL common-mode range is ±30V in normal mode. RXD is a logic-high when CANH and CANL are shorted or terminated and un-driven. See *Table 9-1*.

Table 9-1 Receiver Truth Table

$V_{ID}=V_{CANH}-V_{CANL}$	BUS STATE	RXD
$V_{ID} \geq 0.9V$	Dominant	Low
$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
$V_{ID} \leq 0.5V$	Recessive	High
Open ($V_{ID} \approx 0V$)	Open	High

9.4 Transmitter

The transmitter converts a single-ended input signal (TXD) from the local CAN controller to differential outputs for the bus lines CANH and CANL. The truth table for the transmitter is provided in *Table 9-2*. CANH and CANL outputs are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

Table 9-2 Transmitter Truth Table (When Not Connected to the Bus)

V_{CC}	INPUT	TXD LOW TIME	OUTPUT		BUS STATE
	TXD		CANH	CANL	
Power Up	Low	< t_{TXD_DTO}	High	Low	Dominant
	Low	> t_{TXD_DTO}	$V_{ISO}/2$	$V_{ISO}/2$	Recessive
	High or Open	X	$V_{ISO}/2$	$V_{ISO}/2$	Recessive
Power Down	X	X	Hi-Z	Hi-Z	Hi-Z

X = Don't care, Hi-Z = high-impedance.

9.5 Protection Functions

9.5.1 Signal Isolation

The CA-IS2062 devices integrated digital galvanic isolators using Chipanalog's capacitive isolation technology based on the ON-OFF keying (OOK) modulation scheme, allow data transmission between the controller side and cable side of the transceiver with different power domains. Also, the power isolation is achieved with an integrated DC-DC convertor to generate a regulated 5V supply for the cable-side.

9.5.2 Thermal Shutdown

If the junction temperature of the CA-IS2062 device exceeds the thermal shutdown threshold $T_{J(shutdown)}$ (165°C, typ.), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.5.3 Current-Limit

The CA-IS2062 protect the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. However, this will cause large supply current and dissipation. Thermal shutdown further protects the devices from excessive temperatures that may result from a short circuit. The transmitter returns to normal operation once the short is removed.

9.5.4 Transmitter-Dominant Timeout

The CA-IS2062 devices feature a transmitter-dominant timeout (t_{TXD_DTO}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t_{TXD_DTO}, the transmitter is disabled, releasing the bus to a recessive state. After a dominant timeout fault, the transmitter is re-enabled when receiving a rising edge at TXD. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. So the minimum transmitted data rate can be calculated as: 11 bits/t_{TXD_DTO} = 11 bits / 2ms = 5.5kbps. The transmitter-dominant timeout limits the minimum possible data rate of the CA-IS2062 to 5.5kbps.

10 Application Information

CAN interface has been a very popular serial communication standard in the industry and automotive applications due to its excellent prioritization and arbitration capabilities. In systems with different voltage domains, isolation is typically used to protect the low voltage side from the high voltage side in case of any faults. The CA-IS2062x provide complete isolated solution for these kind of applications, see Figure10-1, the typical application circuit.

The CA-IS2062x devices can operate up to 1Mbps data rate. However, the maximum data rate is limited by the bus loading, number of nodes, cable length etc. factors. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum data rate, number of nodes often lower. The ISO11898 Standard specifies a maximum of 30 nodes. However, with careful design, and consider of high input impedance of the CA-IS2062x, designers can have many more nodes (up to 110) on the CAN bus.

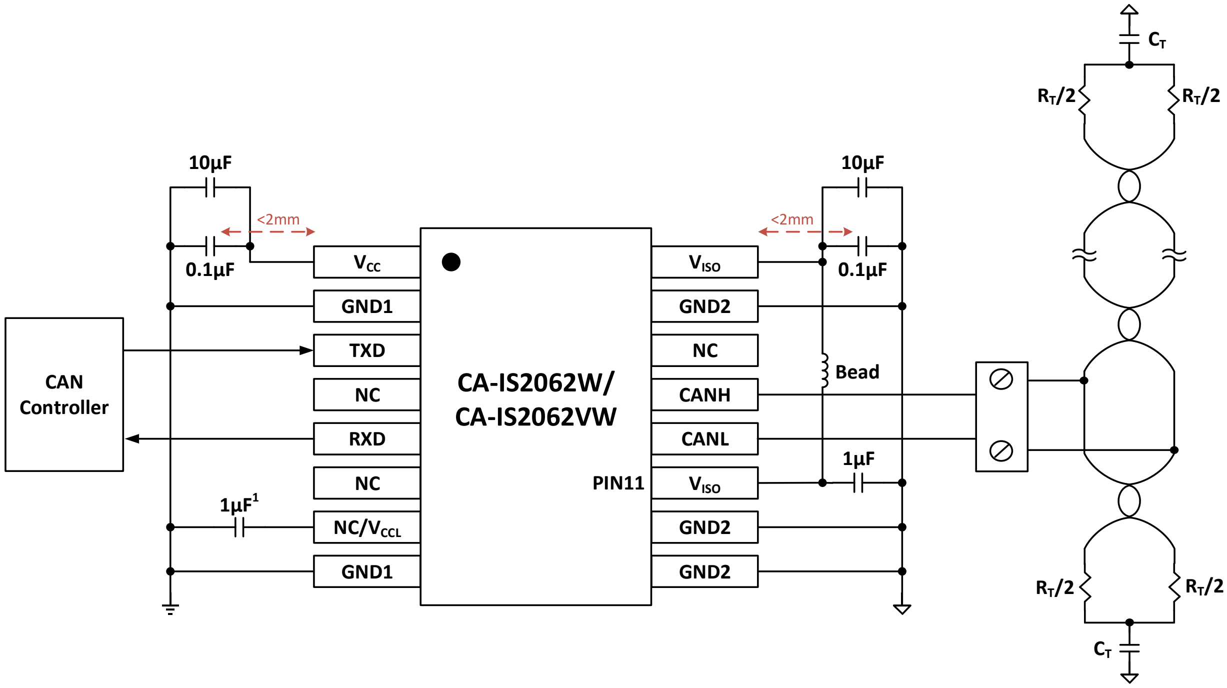


Figure 10- 1 Typical Application Circuit

In multi-drop CAN applications, it is important to maintain a single linear bus of uniform impedance that is properly terminated at each end. A star, ring, or tree configuration should never be used. Any deviation from the end-to-end wiring scheme creates a stub. High-speed data edges on a stub can create reflections back down to the bus. These reflections can cause data errors by eroding the noise margin of the system. Although stubs are unavoidable in a multi-drop system, care should be taken to keep these stubs as short as possible, especially when operating with high data rates. See Figure10-2, the typical CAN bus operating circuit, termination may be a single 120Ω resistor (R_T) at the end of the bus, either on the cable or in a terminating node; or split termination, the two 60Ω termination resistors in parallel may be used if filtering and stabilization of the common mode voltage of the bus is desired.

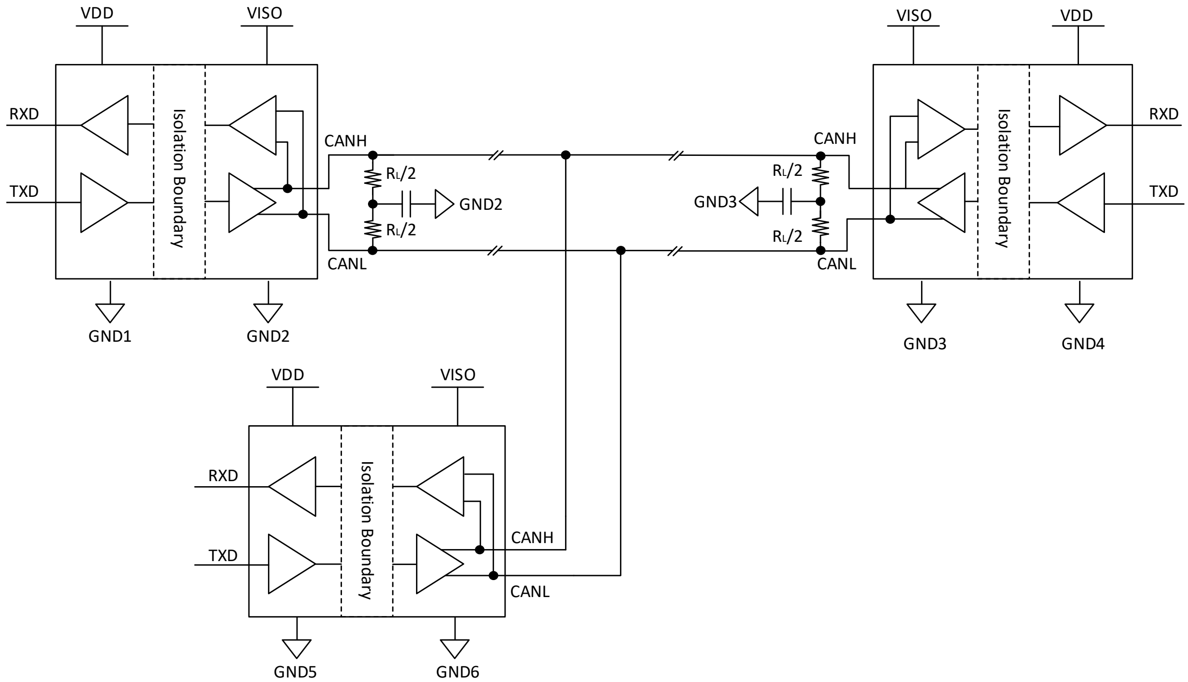


Figure 10- 2 Typical CAN Bus Operating Circuit

To ensure reliable operation at all data rates, it is strongly recommended to bypass V_{CC} and V_{ISO} with 0.1µF||10µF low-ESR ceramic capacitors to GND1 and GND2 respectively. Place the bypass capacitors as close to the power supply input/output pins as possible. The PCB designer should follow some critical recommendations in order to get the best performance from the design. For the high-speed operating digital circuit boards, we recommend to use the standard FR-4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals. For harsh industrial environments, external protection might be necessary to protect the CAN transceiver during normal operation. If the 10µF ceramic capacitor can't be placed for some reason, a 4.7µF ceramic capacitor is the minimal value needed. Place the 10µF ceramic close to V_{CC} and V_{ISO} pins and keep distance within 2mm. The input/output ceramic capacitor and the IC must be placed on the same PCB layer and connected without any vias to reduce parasite. The recommended PCB layout of CA-IS2062VW is shown in Figure10-3. For the logic supply input, we recommend to use a 1µF ceramic capacitors with X5R or X7R between V_{CCL} pin and GND1. V_{ISO}(PIN11) is power pin for CAN module inside, place a 1µF ceramic capacitors as close as possible to this pin.

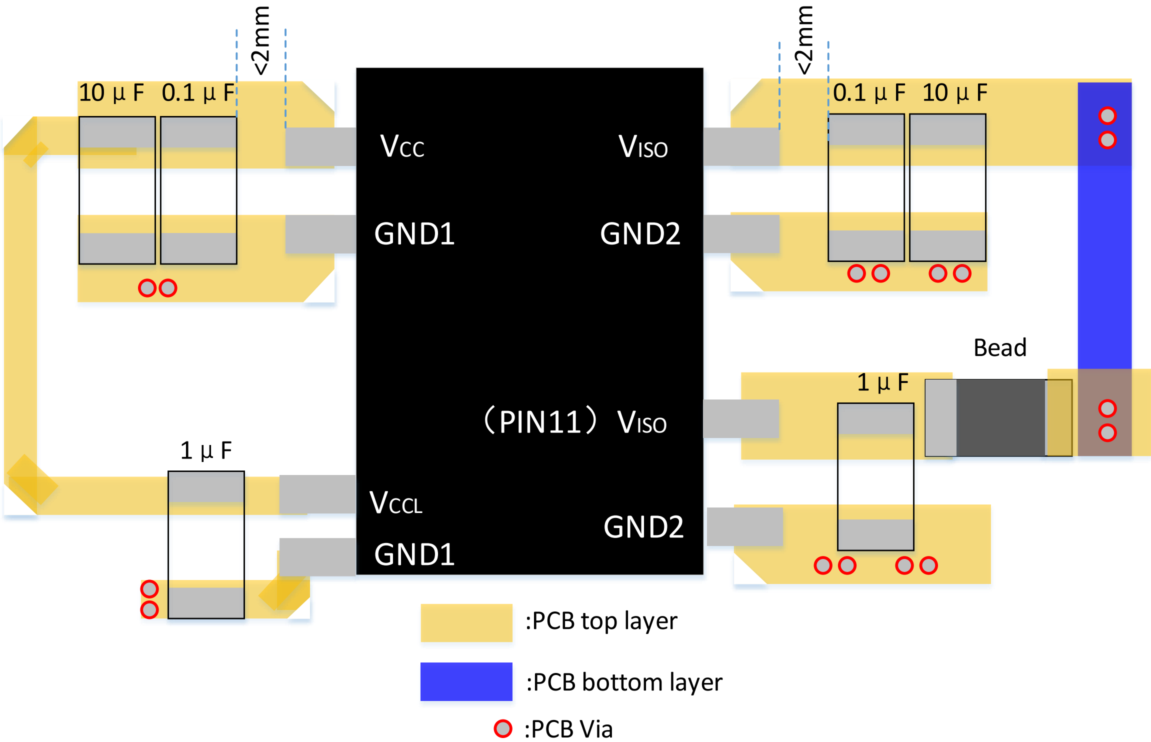
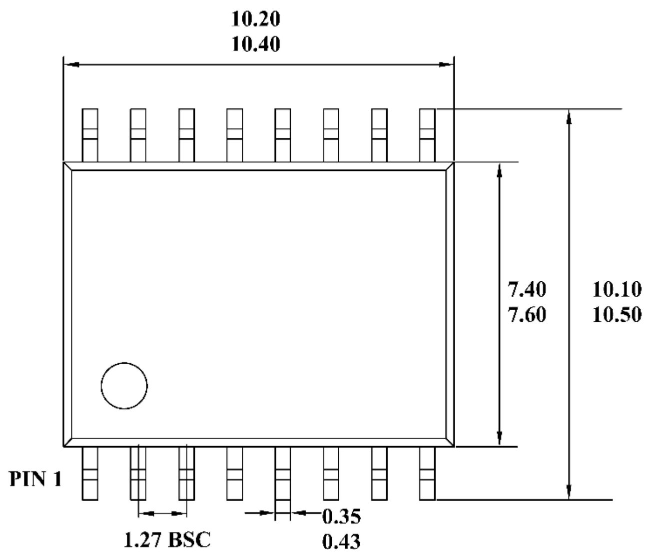


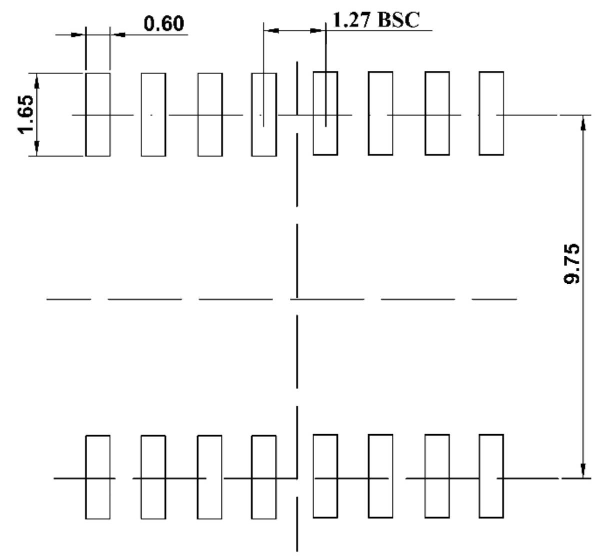
Figure 10- 3 Recommended PCB layout of isolated power

11 Package Information

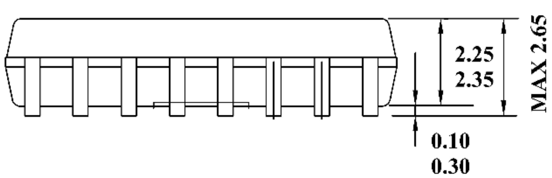
Wide-body SOIC16 Package Outline



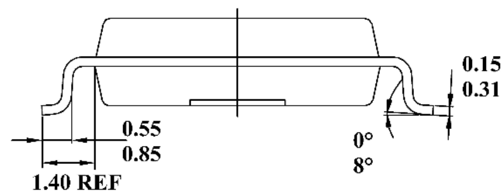
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12 Soldering Temperature (reflow) Profile

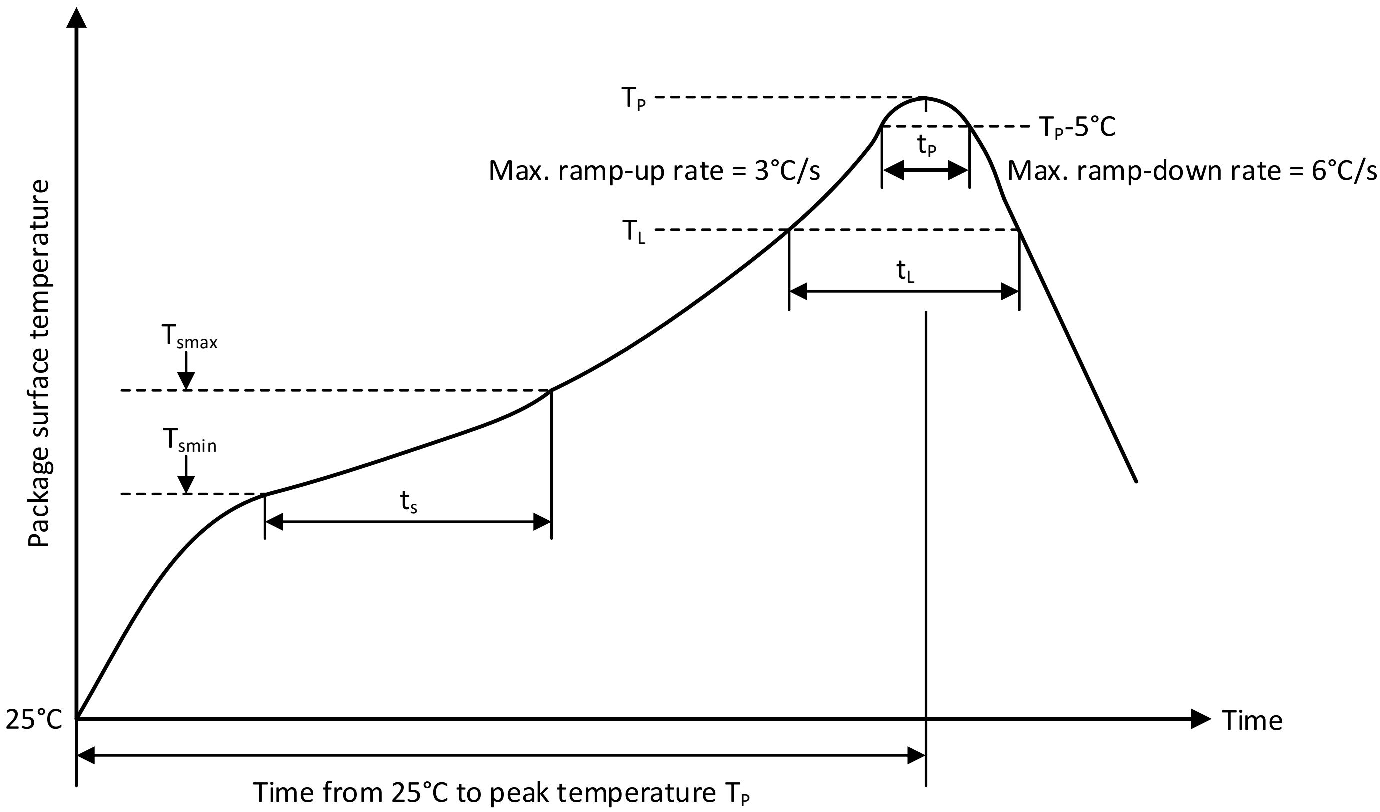


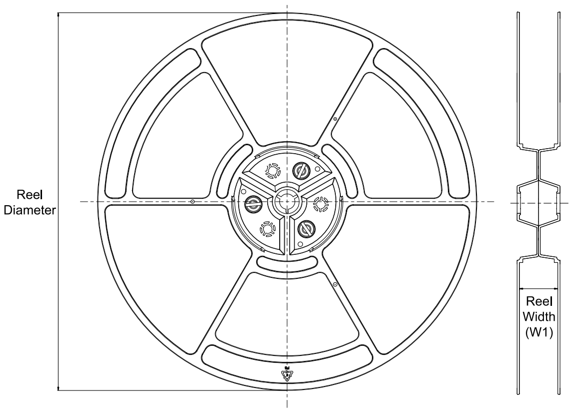
Figure. 12-1 Soldering Temperature (reflow) Profile

Tab.12- 1 Soldering Temperature Parameter

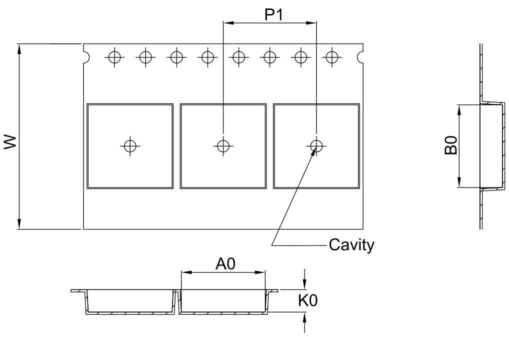
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

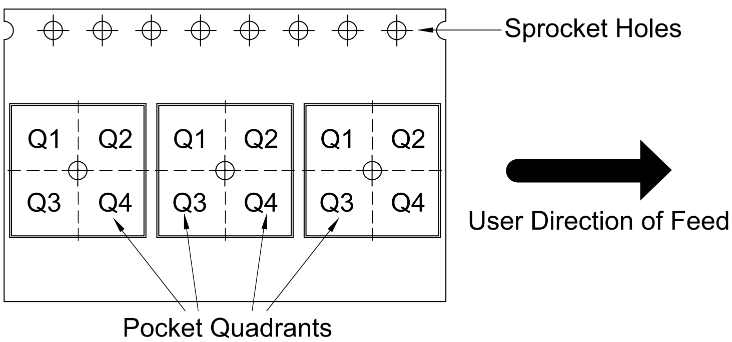


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS2062W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS2062VW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

14 Important Statement

The above information is for reference only and intended to help Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.

http://www.chipanalog.com