GX21M15（GX75B）

Digital temperature sensor with watchdog function

Product data sheet

GXCAS TECHNOLOGY

1. summary

The GX21M15 is a temperature-to-digital converter that uses an on-chip bandgap temperature sensor and Σ-Δ A/D conversion technology, with overheat detection output. The GX21M15 includes a series of data registers: configuration registers (Conf) that store device settings such as operating mode, OS operating mode, OS polarity, and OS fault queue; see Section 7 "Function Description" for details. Temperature registers (Temp) store digital temperature data, and setting point registers (Tos and Thyst) store programmable overheat shutdown thresholds and hysteresis limits, which can communicate with the controller via a 2-wire serial I²C bus interface. The device also provides an open-drain output (OS) that can be activated when the temperature exceeds the programmed threshold limit. The temperature sensor has three logic address pins, allowing up to eight devices to be connected on the same bus without address conflicts.

GX21M15 can be configured for different operating modes. It can be set to normal mode for regular environmental temperature monitoring, or to shutdown mode to minimize power consumption. The OS output can operate in either of two optional modes: OS comparator mode or OS interrupt mode. Its valid output state can be configured as high or low level. The number of consecutive faults that trigger the OS output fault queue and the setpoint limit threshold are both programmable.

The temperature register always stores 11-bit binary two's complement data, with a temperature resolution of 0.125 . This high temperature resolution is particularly useful for applications that require precise measurement of thermal drift or thermal escape. When accessing the GX21M15, it does not interrupt the ongoing temperature conversion (i.e., the I2C bus part is completely independent of the Σ-Δ converter part) and allows continuous access to the GX21M15 without waiting for communication time, even during a single temperature conversion period. However, this does not prevent the device from using the new temperature conversion results to update the temperature register. Once the temperature register is updated, the new conversion result can be used immediately.

GX21M15 When powered on, it is in normal working mode, that is, OS is in comparator mode, temperature threshold is 80 and lag value is 75 , so it can be used as an independent thermostat with those predefined temperature set points.

2. feature

- The pins are fully compatible with industry standard LM75 and LM75A pins, providing a temperature resolution of 0.125 and a power supply range of 2.8V to 5.5V
- I2C bus interface, up to 8 devices on the same bus
- Power supply voltage range: 2.8 V to 5.5 V
- The temperature range is-55 to +125
- The frequency range is from 20 Hz to 400 kHz and has a bus fault timeout function to prevent bus hangup
- Provides an 11-bit ADC with a temperature resolution of 0.125
- Temperature accuracy:
  - 0 to +50 : ±0.5

- -25 to + 100 : ±1
- -55 to + 125 : ±1.5

- Programmable alarm temperature threshold and hysteresis value

- The power supply current in the off mode is 0.1μA to achieve energy saving
- It can be used as a thermostat when powered on
- ESD protection exceeds JESD22-A114 4500 V HBM and JESD22-C101 1000 V CDM
- JESD78 completed the latch test of more than 100 mA according to the JEDEC standard
- Small 8-pin package types: SOP8, MSOP8/TSSOP8

3. apply

- System thermal management
- IBM PC
- ED
- ICU

4. Order information

Table 1. Order information

Product model	Top surface marking	Package		
		Name	Description	Edition
GX21M15	GXCAS 21M15 xxyy0z	SOP8	Small size plastic package: 8 leads	V2.0
GX21M15U	GXCAS 21 M15U xxyyD0z	MSOP8	Thin plastic shrinkage small size form packaging: 8 leads	V2.0

5. assumption diagram

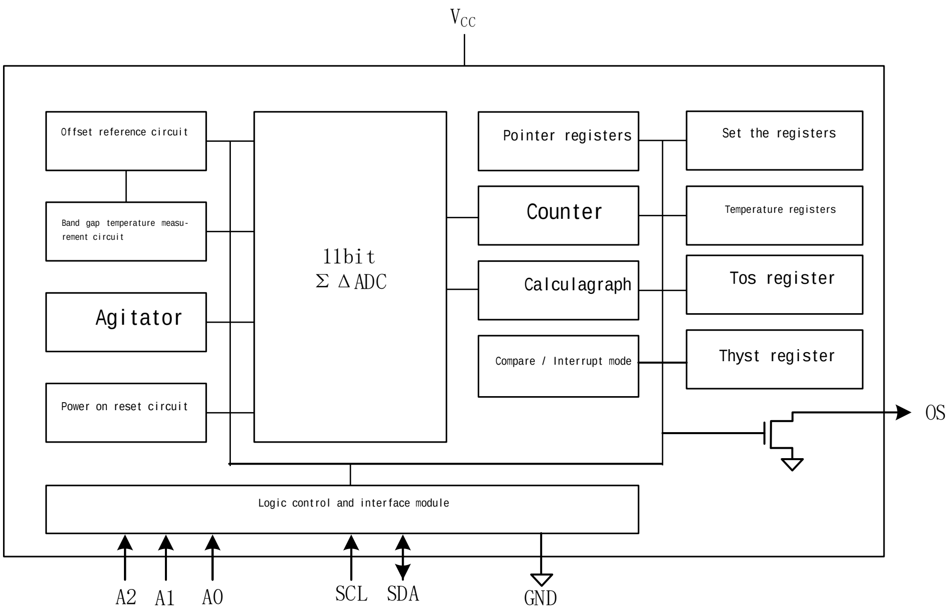
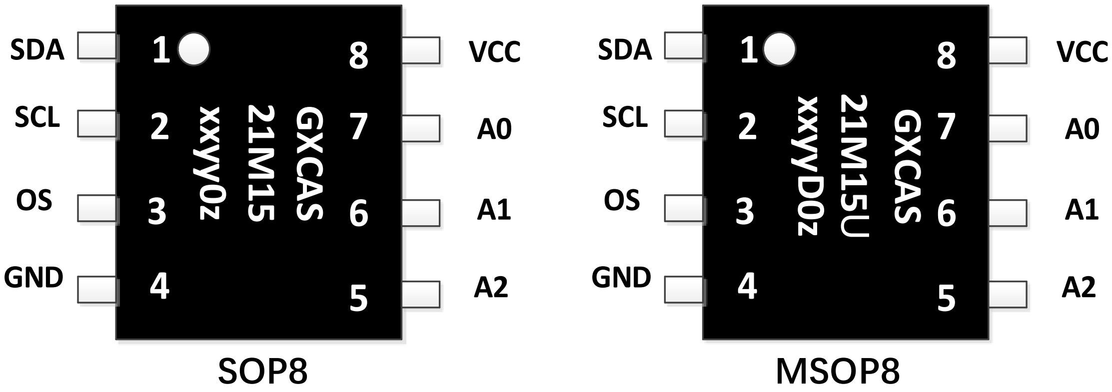


Figure 1. Chip structure diagram

6. Pin information

6.1 Pin distribution



6.2 Pin description

Table 2. Pin description

Pin name	Pin	Description
SDA	1	Digital I/O, I2C bus bidirectional data line; open drain output.
SCL	2	Digital input, I2C bus clock input.
OS	3	Overtemperature protection/output interruption; open drain.
GND	4	Ground, connected to the system ground
A2	5	Digital input, user configures address bit 2.
A1	6	Digital input, user configures address bit 1.
A0	7	Digital input, user configures address bit 0.
V_{CC}	8	Power port

7. functional description

7.1 task description

GX21M15 Use an on-chip bandgap temperature sensor to measure the device temperature with a resolution of 0.125 , and store the 11-bit binary number generated by the 11-bit A-D conversion in the device temperature register. This temperature register can be read at any time by the controller on the I2C bus. Reading the temperature data does not affect the ongoing temperature conversion during the read operation.

The device can be set to operate in normal or sleep mode. In normal operation mode, the temperature is converted every 100ms, and the temperature register is updated at the end of each conversion. During a conversion cycle (Tconv) of about 100ms, the device only needs to work for 10ms to complete the temperature-to-data conversion, known as the "temperature conversion time" (tconv(T)). The remaining time is spent in idle mode. This feature significantly reduces the device's power consumption. In sleep mode, the device is idle, data conversion is disabled, and the temperature register retains the latest result; however, the device's I2C bus interface remains active, allowing for register write/read operations. By programming the B0 bit of the configuration register, the device's operating mode can be controlled. Temperature conversion is initiated when the device powers on or resumes from sleep mode to normal mode.

In addition, at the end of each transition in normal mode, the temperature data in the temperature register is automatically compared with the data in the overtemperature shutdown register Tos (or Tth(ots)) and the data stored in the lag register Thyst (Thyst) to determine the output state of the device accordingly. The Tos and Thyst registers of the device are read/write capable and operate using 9-bit binary digital data. To match this 9-bit operation, the temperature register only uses its 11-bit data, specifically the 9 MSB bits, for comparison.

The comparison operation mode of the output response of the OS port is determined by the B1 bit of the configuration register, and the user-defined fault queue is determined by the configuration bits B3 and B4.

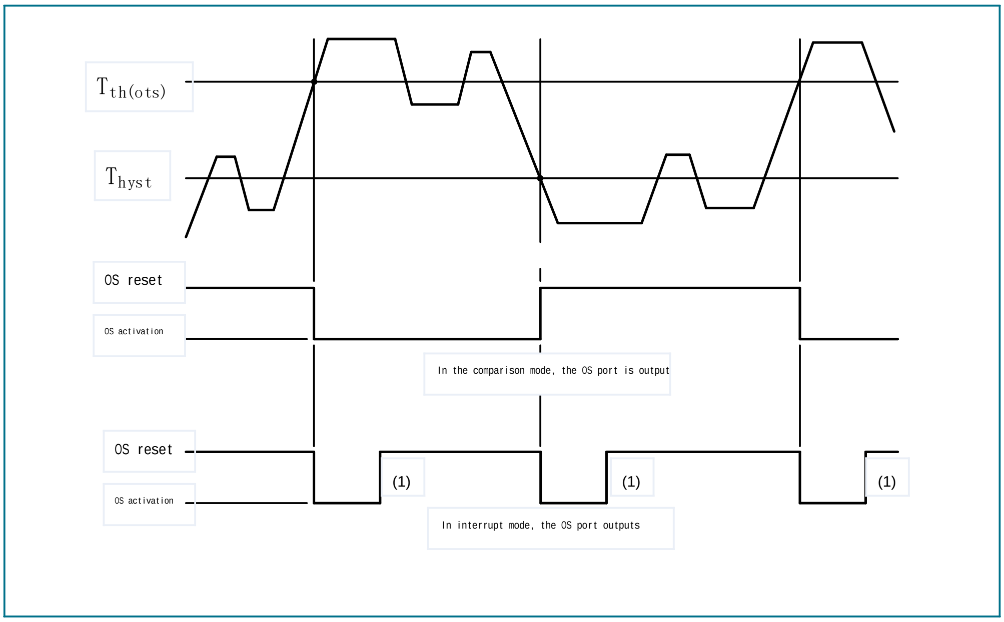
In comparator mode, the output behavior of the OS port is similar to that of a thermostat. It activates when the temperature exceeds Tth (ots) and resets when the temperature drops below Thyst. Reading a register or placing the chip in sleep mode does not change the output state of the chip. In this mode, the OS output can be used to control cooling fans or thermal switches.

In interrupt mode, the output behavior of the OS port is used for thermal interrupts. When the device is powered on, it is only activated first when the temperature exceeds Tth (ots); then it will remain in this state indefinitely until reset by reading any register. Once the OS output is activated through crossing Tth (ots) and then reset, it can only be reactivated when the temperature drops below Thyst; after that, it will remain in the active state indefinitely until reset by reading any register. The operating system interrupt operations will continue in the following order: Tth (ots) trip, Reset, Thyst trip, Reset, Tth (ots) trip, Reset, Thyst trip, Reset, etc. Setting the bit 0 of the configuration register to put the device into sleep mode also resets the operating OS output.

In both the comparator mode and the interrupt mode, the OS output is activated only when multiple consecutive faults defined by the fault queue are met. The fault queue is programmable and stored in two bits B3 and B4 of the configuration register. Additionally, by setting the corresponding bits B2 of the configuration register, the valid state of the OS output can be selected as high or low.

When the chip is powered on, the device enters normal mode, Tth(ots) is 80 , Thyst is 75 , OS activation state is low, and the fault queue is equal to 1. The first conversion is completed within about 100ms after power on, and the temperature reading data is not available before this conversion is completed.

The temperature response of the OS port is shown in Figure 6



(1) The OS resets by reading the registers or configuring the chip into sleep mode. Assume that the fault queue is in each

It is satisfied at the intersection of Tth (ots) and Thyst.

Figure 6. OS port output diagram

7.2 I2 C bus interface

GX21M15 can connect to a compatible 2-wire serial interface, I2C bus, and function as a slave device under the control of a controller or master device, using two device terminals SCL and SDA for communication. It is necessary to provide signals through these terminals to write data from terminal SDA/SDA to the controller. Note that if the pull-up resistors on the I2C bus are not installed according to the requirements of the I2C bus, each of these two ports will require an external pull-up resistor of approximately 10K. For details on the bus communication protocol, see Section 7.10.

7.2.1 The total number of threads exceeded the timeout

If the SDA remains at a low level for more than tto (minimum 75ms/13.3Hz; ensure minimum

5ms/20Hz), GX21M15 will reset to idle state (SDA is released) and wait for new start conditions.

This ensures that the GX21M15 does not hang up the bus when a transmission conflict occurs.

7.3 From the machine address

The GX21M15 on the I2C bus has its slave address determined by the logic of pins A2, A1, and A0. Each of these pins is typically connected to GND (logic 0) or VCC (logic 1). These pins represent the three least significant bits (LSBs) of the device's 7-bit address. The other four most significant bits (MSBs) of the address data are forcibly set to "1001" through internal wiring within the GX21M15. See Table 4

The complete address of the device, and indicate that up to 8 devices can be connected to the same bus without address conflict

There is no internal bias for the input pins SCL, SDA and A2 to A0, so they should not be left floating in any application.

Table 4. List of addresses

1 = Vcc; 0 = GND.

MSB						**LSB**
1	0	0	1	A2	A1	A0

7.4 Register list

GX21M15 There are four data registers next to the pointer register, as shown in Table 5. Table 5 also shows the pointer value, read/write capability, and default content when the register is powered on

Table 5. List of registers

Register name	Pointer value	Read/write	Power on by default	Description
Conf	01h	Read/write	00h	Configuration register: Contains an 8-bit data byte; used to set the operating conditions of the chip; default value is 0.
Temp	00h	Read only	n/a	Temperature register: Contains 28-bit data bytes; used to store the measured temperature data.
Tos	03h	Read/write	5000h	Overtemperature shutdown register: contains 28-bit data bytes to store the Tth (ots) value; default value = 80 .
Thyst	02h	Read/write	4B00h	Backlog register: Contains 28-bit data bytes; used to store the Thyst value; default value = 75

7.4.1 Pointer registers

The pointer register contains 18-bit data, where 2 of the LSB bits represent the pointer values of the other 4 registers, and the remaining 6 MSB bits are equal to 0, as shown in Table 6 and Table 7. The user cannot access the pointer register, but it selects data registers for write/read operations by including pointer data bytes in the bus command.

Table 6 Pointer registers

B7	B6	B5	B4	B3	B2	B[1:0]
0	0	0	0	0	0	Pointer value

Table 7 Pointer value

B1	B0	Register
0	0	Temperature register (Temp)
0	1	Configuration registers (Conf)
1	0	Backlog Register (Thyst)
1	1	Overtemperature shutdown register (Tos)

Because the pointer byte is latched into the pointer register when executing bus commands (including pointer bytes), the pointer byte read from the GX21M15 may or may not be included in the statement. When reading the register that was last preset by the pointer, the pointer byte does not need to be included. However, when reading a different register than the previous one, the pointer byte must be included. Nevertheless, during write operations on the GX21M15, the pointer byte must always be included in the statement. For details on the bus communication protocol, see Section 7.10.

When powered on, the pointer value is equal to 00 and the temperature register is selected; then, the user can read the temperature data without specifying the pointer byte.

7.4.2 Set the registers

The configuration register (Conf) is a write/read register containing an 8-bit non-complement data byte that is used to configure the chip for different operating conditions. Table 8 shows the bit allocation of this register.

Table 8. Configuration registers

*Legend: * = default value.*

Position	Symbol	Authority	Price	Description
B[7:5]	reserved	Read/write	000*	Reserved for use by the manufacturer; it should be kept at zero during normal operation
B[4:3]	OS_F_QUE[1:0]	Read/write		OS fault queue programming
			00*	Queue value = 1
			01	Queue value = 2
			10	Queue value = 4
			11	Queue value = 6
B2	OS_POL	Read/write		OS polarity selection
			0*	The OS activates the output at a low level
			1	The OS activates the output at a high level
B1	OS_COMP_INT	read/write		OS mode selection
			0*	OS Compare patterns
			1	OS Interrupt mode

B0 SHUTDOWN Read/write	Chip working mode selection	
	0*	normal
	1	sleep

7.4.3 Temperature registers

The temperature register (Temp) stores the results of temperature measurements or monitoring at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes, consisting of one most significant byte (MSByte) and one least significant byte (LSByte). However, only 11 bits of these two bytes are used to store temperature data in a 2's complement format, with a resolution of 0.125 . Table 9 shows the bit arrangement of the temperature data in the data bytes.

Table 9. Temp register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X

When reading the temperature register, all 16 bits of the two data bytes (MSByte and LSByte) are provided to the bus and must be collected by the controller to complete the bus operation. However, only the 11 highest significant bits should be used; the 5 lowest significant bits of LSByte are zero and should be ignored. One method for calculating the temperature value from the 11-bit temperature data is:

1. If the temperature data MSByte is D10=0, then the temperature is positive and

   The temperature value is ( ) =+ (temperature data) ×0.125 ;

2. If the temperature data MSByte is D10=1, the temperature is negative and

   Temperature value ( ) = (the parity code of the two temperature data) × 0.125 .

Table 10 shows an example of temperature data and temperature values.

Table 10. Temperature register values

A 11-bit binary number	Hexadecimal number	Decimal number	Temperature scale
011 1111 1000	3F8	1 016	+127.000℃
011 1111 0111	3F7	1 015	+126.875℃
011 1111 0001	3F1	1 009	+126.125 ℃
011 1110 1000	3E8	1 000	+125.000℃
000 1100 1000	0C8	200	+25.000 ℃
000 0000 0001	001	1	0.125℃
000 0000 0000	000	0	0.000℃
111 1111 1111	7FF	–1	–0.125 ℃
111 0011 1000	738	–200	–25.000℃
110 0100 1001	649	–439	–54.875℃
110 0100 1000	648	–440	–55.000℃

For the application of 9-bit temperature data to replace industrial standard XX 75, only two bytes are required, using the 9 MSB bits while ignoring the 7 LSB bits. The definition of 9-bit temperature data with a resolution of 0.5 is identical to that of standard XX75 and is similar to the Tos and Thyst registers.

GX21M15

The MSB of the temperature can also be read using a single byte read command. The temperature resolution will then be changed to 1.00 .

7.4.4 Overtemperature shutdown threshold (Tos) and hysteresis (Thyst) registers

These two registers are write/read registers, also known as setpoint registers. They store user-defined temperature limits, referred to as the overtemperature shutdown threshold (Tth(ots)) and the hysteresis temperature (Thyst), for use in device watchdog operations. At the end of each conversion, the temperature data is compared with the data stored in these two registers to set the state of the OS end output; see Section 7.1.

Each setpoint register contains two 8-bit data, consisting of a MSByte and a LSByte, similar to the temperature register. However, only 9 bits out of the two bytes are used to store the setpoint data in binary form, with a resolution of 0.5 . Tables 11 and 12 show the bit arrangement of Tos, data, and Thyst data in the data byte.

Note that because only 9 bits of data are used in the set value register, the device only uses the 9 MSB of temperature data for data comparison.

Table 11. Overtemperature shutdown threshold register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X

Table 12. Backlog of deposits

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X

When reading the set value register, all 16 bits are provided to the bus and must be collected by the controller to complete the bus operation. However, only the nine highest significant bits should be used and the seven lower bits of LSByte equal zero and should be ignored

summary.

Table 13 shows an example of setting data and values.

Table 13.Tos and Thyst set the data and values

Binary number	Hexadecimal number	Decimal number	Temperature scale
0 1111 1010	0FA	250	+125℃
0 0011 0010	32	50	+25℃
0 0000 0001	001	1	+0.5℃
0 0000 0000	000	0	0℃
1 1111 1111	1FF	-1	-0.5℃
1 1100 1110	1CE	-50	-25.0℃
1 1001 0010	192	-110	-55.0℃

7.5 OS output and polarity

The OS end is an open-drain output, its state indicating the result of the device watchdog operation described in Section 7.1. To observe this output state, an external pull-up resistor is required. The resistor should be as large as possible, up to 200 kΩ, to minimize temperature reading errors caused by internal heating due to high OS notch current.

By programming the bit B2 (OS_POL) of register Conf, you can set the OS output active state to high or low: Set the bit OS_POL to logic 1 to select a high level for the OS activation output, and set the bit B2 to logic 0 to set the OS activation output to a low level. When powered on, the bit OS_POL is equal to logic 0, and the OS activation output is at a low level.

7.6 OS comparison and interrupt mode

As mentioned in Section 7.1, the OS output response is the result of comparing temperature register data with data from the Tos and Thyst registers, depending on the selected operating system mode: OS comparison or interrupt mode. The OS mode can be selected by configuring the bit B1 (OS_COMP_INT) of the Conf register: setting the OS_COMP_INT bit to logical 1 selects OS interrupt mode, and setting it to logical 0 selects OS comparison mode. At power-on, the OS_COMP_INT bit is initially set to logical 0, and OS comparison mode is selected.

The main difference between these two modes lies in the following: In comparison mode, when the temperature exceeds Tth (ots), the OS activates; it resets when the temperature drops below Thyst. Reading the register or putting the chip into sleep mode does not change the state of the OS output. In interrupt mode, once activated by exceeding Tth (ots) or falling below Thyst, the OS output remains active indefinitely until the register is read, at which point the OS output is reset.

The temperature threshold Tth (ots) and Thyst must satisfy Tth (ots)>Thyst. Otherwise, the OS output state will be undefined.

7.7 OS fault queue

The fault queue is defined as the number of faults that must occur continuo-usly in order to activate the OS output. To avoid false activation due to noise, the fault queue is also defined as the number of consecutive convers-ions that return the temperature trip when the data conversion is completed.

The value of the fault queue can be selected by programming two bits, B4 and B3 (OS_F_QUE[1:0]), in the register Conf. Note that the programmed data is not the same as the fault queue value. Table 14 shows the one-to-one relationship between them. At power-on, the fault queue data =0 and the fault queue value = 1.

Table 14. List of fault queues

Fault queue data		The fault queue value
OS_F_QUE[1]	**OS_F_QUE[0]**	Decimal system
0	0	1
0	1	2
1	0	4
1	1	6

7.8 Sleep patterns

The operating mode is selected by setting the bit B0 (sleep) of the programmable register Conf. Setting B0 to logic 1 will put the device into sleep mode. Resetting the B0 bit to logic 0 will return it to normal mode.

In sleep mode, approximately 0.1uA of current is consumed; temperature conversion stops, but the I2C bus interface remains active and can perform register write/read operations. After entering sleep mode, the chip output will remain unchanged in comparator mode and reset in interrupt mode.

7.9 Power on defaults and power on reset

GX21M15 Power-on default state:

- ? Normal working mode
- ? OS Comparison Mode
- • $T_{th(ots)}$ = 80 ℃
- • T_{hys} = 75℃
- ? The OS output is activated at a low level
- ? Pointer register value 00 (temperature register)

When the power supply voltage drops below about 1.0V (POR) and remains above for more than 2us, then rises again, the chip will reset to the power-on default state.

7.10 Register read/write protocol

Communication between the host and the GX21M15 must strictly follow the rules defined by the I2C bus management. The protocol for GX21M15 register read/write operations follows the following definitions, as shown in Figures 7 to 12:

1. Before communication, the I2C bus must be idle or not busy. This means that the SCL and SDA lines must be released by all devices on the bus and pulled high through the bus pull-up resistor.
2. The host must provide the SCL clock pulses required for communication. Data is transmitted in a sequence of nine SCL clock pulses for every eight bits of data, followed by one bit of ACK.
3. During data transfer, in addition to the start and stop signals, the SDA signal must be stable when the SCL signal is high. This means that the SDA signal can only change during the low duration of the SCL line.
4. S: Start signal, which is sent by the host to start communication. When SCL is high, SDA changes from high to low.
5. RS: Restart signal, which is the same as the start signal, is used to start the read command after the write command.
6. P: Stop signal, which is issued by the host to stop communication. SDA changes from low to high and SCL is high. Bus release.
7. W: Write position, when the write/read position in the write command is 0.
8. R: Read bit, when the write/read bit in the read command is 1.
9. A: The slave ACK bit is returned by the GX21M15. If it works properly, it is 0; if not, it is 1. The master must release the SDA line during this period so that devices on the bus can control the SDA line.
10. A': The host ACK bit is not returned by the slave but is issued by the host or the host when reading 2 bytes of data. Within this clock cycle, the host must set the SDA line to low to inform the device that the first byte has been read, so that the device can provide the second byte on the bus.
11. NA: No ACK position. During this clock cycle, both the device and the host release the SDA line at the end of the data transfer, allowing the host to generate a stop signal.
12. In the write protocol, data is sent from the host to the device, and the host controls the SDA line except for the clock cycle when the device sends a device confirmation signal to the bus.
13. In the read protocol, data is sent from the device to the bus, and the host must release the SDA line during the time when the device provides data to the bus and controls the SDA line, except for the clock cycle when the host sends a host confirmation signal to the bus.

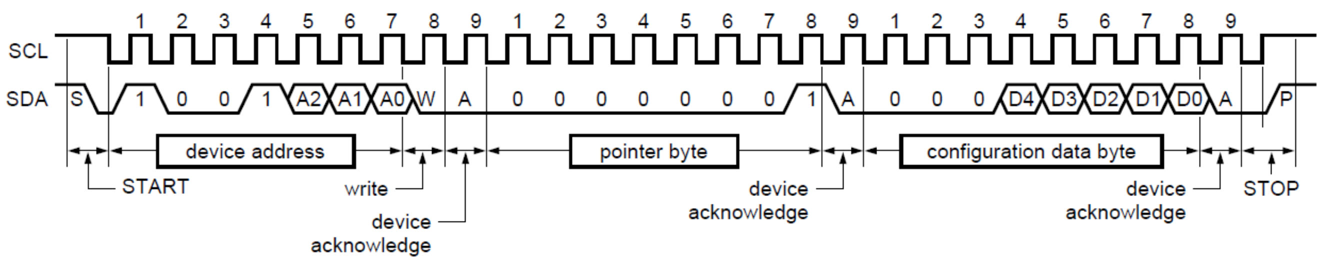


Figure 7. Write configuration registers (1-byte data)

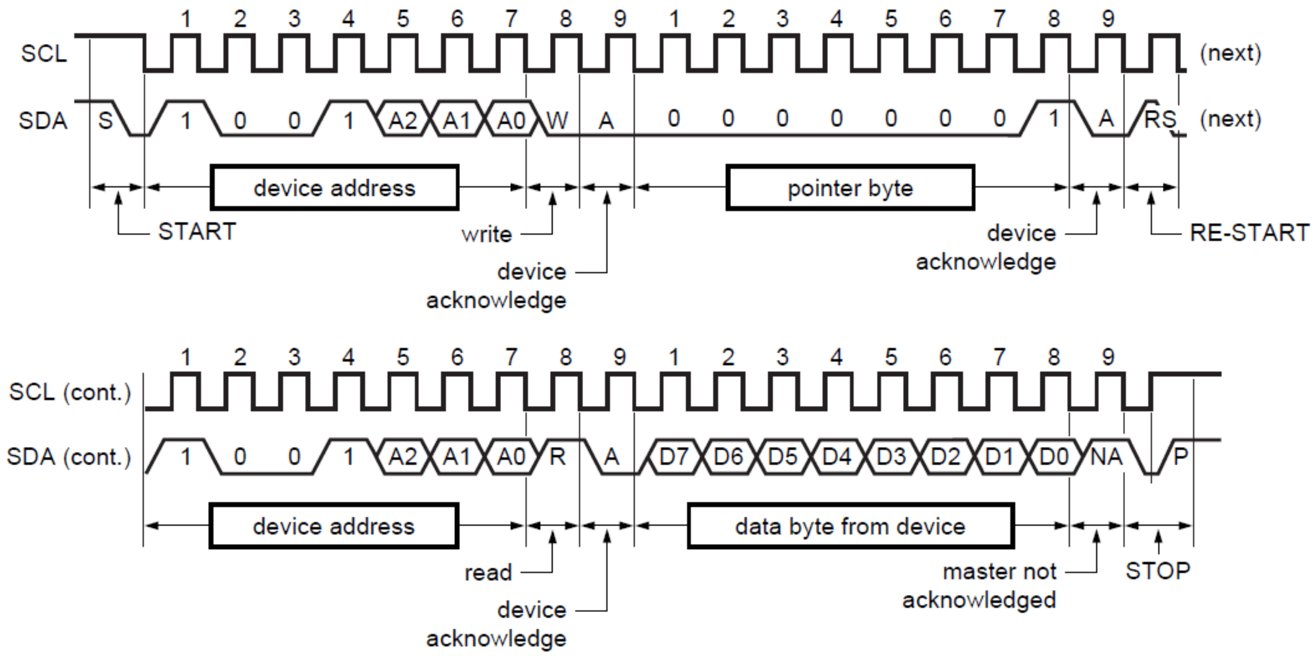


Figure 8. Reading configuration registers (1-byte data)

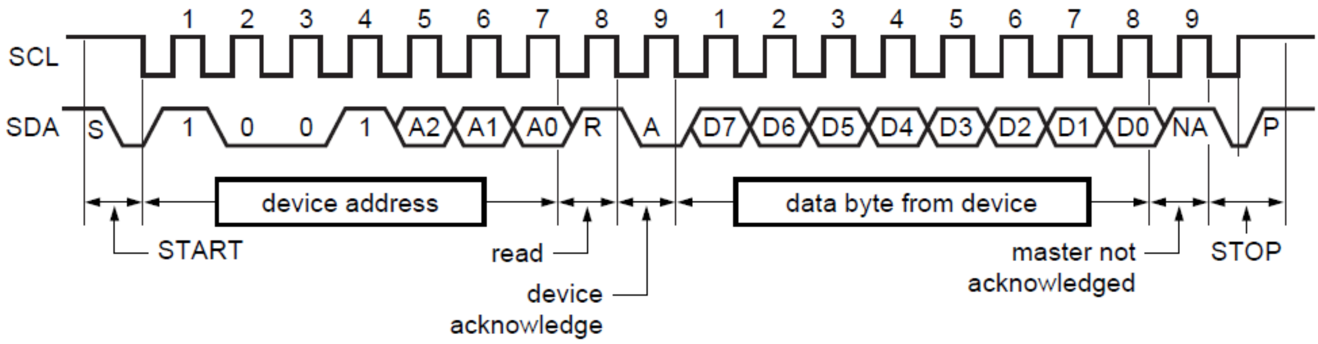


Figure 9. Reading configuration or temperature registers (1-byte data) using preset pointer

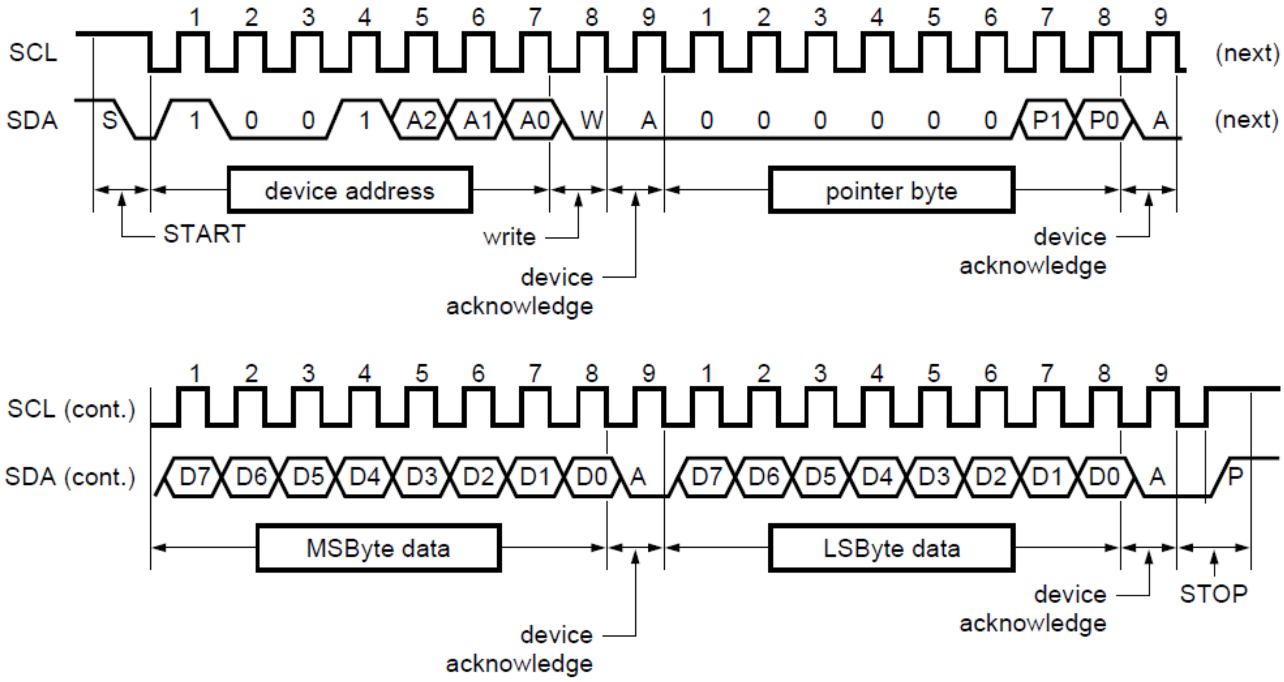


Figure 10. Write to the Tos or Thyst registers (2-byte data)

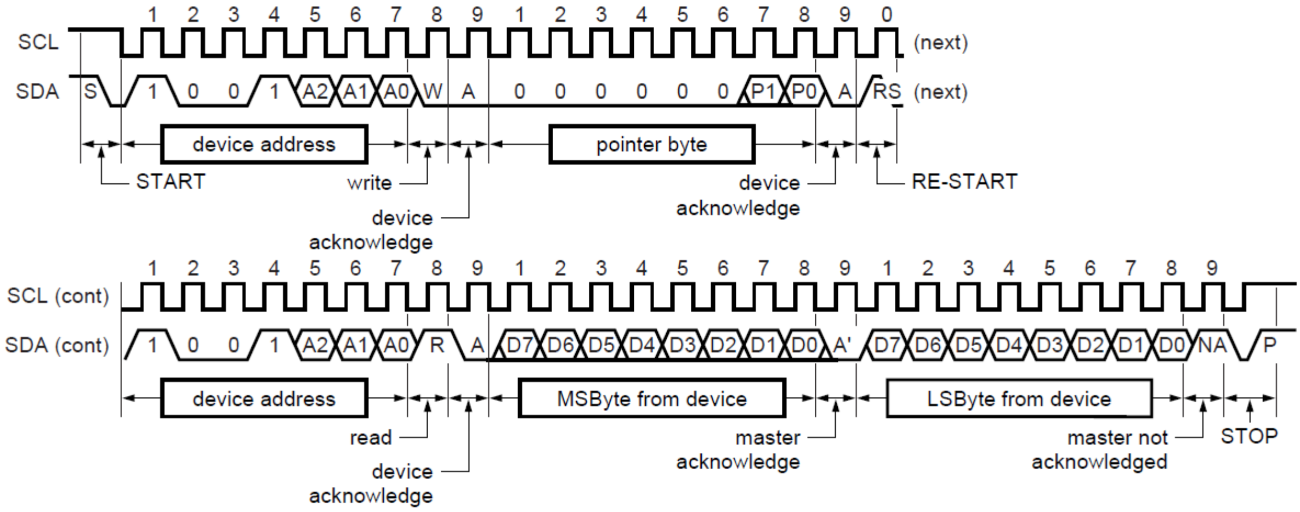


Figure 11. Read temperature, Tos or Thyst registers (2-byte data)

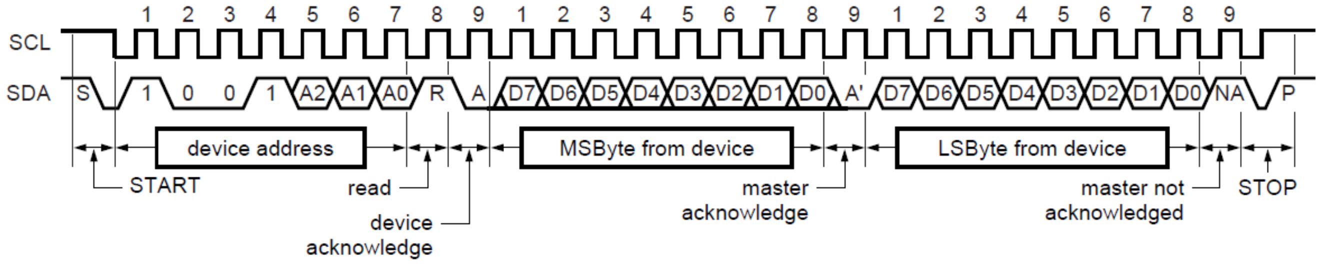


Figure 12. Reading the temperature from the preset pointer, Tos or Thyst registers (2-byte data)

8. application message

8.1 Typical application

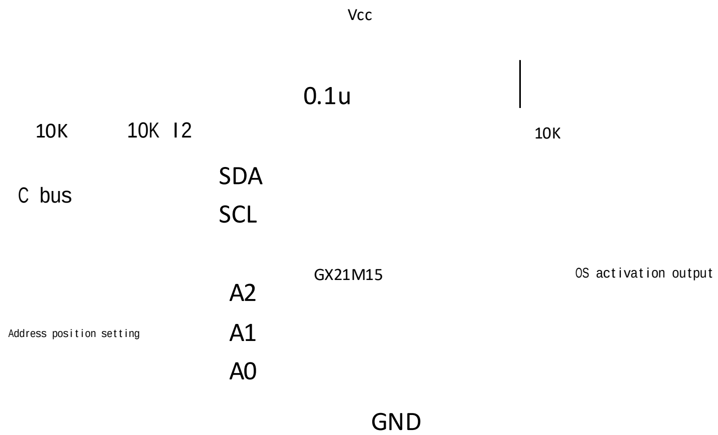


Figure 13. Typical application

8.2 Temperature accuracy

Due to the local channel of the temperature sensor measuring the mold temperature transmitted from its body, it is essential to stabilize and saturate the temperature of the device's main body to provide stable readings. Since GX21M15 operates at low power levels, the thermal gradient in the device package has a minimal impact on measurement accuracy. The accuracy of measurements depends more on the definition of ambient temperature, which is influenced by various factors: the printed circuit board where the device is installed; airflow that contacts the device body (if there is a significant difference between the ambient air temperature and the printed circuit board temperature, the measurement may become unstable due to different thermal paths between the mold and the environment). When the device is fully immersed in a hot bath, the constant-temperature liquid in the hot bath will provide the best temperature environment. A thermocouple inside a sealed end metal tube installed in a constant-temperature air also offers an excellent method for temperature measurement.

To calculate the effect of self-heating, use equation 1 below:

Equation 1 is the formula for calculating self-heating effect:

$$\Delta T = R_{th(j\text{-}a)} \times [(V_{DD} \times I_{DD(AV)}) + (V_{OL(SDA)} \times I_{OL(sink)(SDA)}) + (V_{OL(EVENT)} \times I_{OL(sink)EVENT})] \quad (1)$$

among:

ΔT = Tj-Tamb Tj = The temperature of the junction

Tamb = room temperature Rth (j-a) = package thermal resistance V DD = supply voltage IDD (AV) = average current

VOL (SDA) = SDA Low Output Voltage

VOL (EVENT) = EVENT, low output voltage

IOL (sink) (SDA) = ~~SDA low ou~~tput current

IOL (sink) EVENT = EVENT, low output current

Example of calculation:

Tamb (typical temperature inside a laptop) = 50 ° C

$I_{DD(AV)}$ = 400 μA

V_{DD} = 3.6 V

Maximum $V_{OL(SDA)}$ = 0.4 V

$I_{OL(sink)(SDA)}$ = 1 mA $V_{OL(EVENT)}$ = 0.4 V $I_{OL(sink)EVENT}$ = 3 mA $R_{th(j-a)}$ = 56 °C/W

Self-heating due to power consumption:

$$\Delta T = 56 \times [(3.6 \times 0.4) + (0.4 \times 3) + (0.4 \times 1)] = 56\ °C/W \times 3.04\ mW = 0.17\ °C \quad (2)$$

8.4 noise effect

GX21M15 The design of the device includes achieving good noise resistance:

? There is a low-pass filter on both the SCL and SDA pins;

? The minimum threshold hysteresis voltage of SCL and SDA port input voltage is about 500mV;

? All pins have ESD protection circuits to prevent damage from surges. The ESD protection on the address, OS, SCL, and SDA is grounded. At any supply voltage, the address/OS latch-based device breakdown voltage is typically 11V, while SCL/SDA is usually 9.5V, but this can vary with process and temperature. Since there are no protective diodes from SCL or SDA to VCC, the GX21M15 will not maintain a low level on the I2C line when VCC is not powered. Therefore, if the GX21M15 loses power, it allows the I2C bus to continue operating.

However, when the device is used in a very noisy environment, it is recommended to use good layout practices and additional noise filters:

? Use a decoupling capacitor on the VCC pin.

? Keep the digital path far away from the switching power supply.

? Long distance communication uses appropriate terminals.

? Add capacitors to the SCL and SDA lines to improve the characteristics of the low-pass filter on the bus.

9. extreme

Table 16. Limits

Under the absolute maximum rating system (IEC 60134).

Symbol	Parameter	State	Minimum	Maximum	Unit
V_{CC}	Service voltage		–0.3	+6.0	V
V_I	Input voltage	At the input port	–0.3	+6.0	V
I_I	Input currenton	At the input port	–5.0	+5.0	mA
$I_{O(sink)}$	Output leakage current	OS port	-	10.0	mA
V_O	Output voltage	OS port	–0.3	+6.0	V
T_{stg}	Storage temperature		–65	+150	°C
T_j	Junction temperature		-	150	°C

10. Recommend working conditions

Table 17. Reference work characteristics

Symbol	Parameter	State	Minimum	Typical case	Maximum	Unit
V_{CC}	Service voltage		2.8	-	5.5	V
T_{amb}	Room temperature		–55	-	+125	°C

11. static characteristic

Table 18. Static characteristics

VCC = 2.8 V to 5.5 V; Tamb = -55 oC to +125 oC; unless otherwise specified.

Symbol	Parameter	State	Minimum	Typical [1]	Maximum	Unit
T_{acc}	Temperature accuracy	T_{amb} = −25 °C to +100 °C	−1	-	+1	°C
		T_{amb} = −55 °C to +125 °C	−2	-	+2	°C
T_{res}	Temperature resolution	11-bit digital data	-	0.125	-	°C
$t_{conv(T)}$	Temperature change time	Normal mode	-	10	-	ms
T_{conv}	Switching cycle	Normal mode	-	100	-	ms
$I_{DD(AV)}$	average supply current	Normal mode: I2C bus is not activated	-	80	200	μA
		Normal mode: I2C bus activat-ed; fSCL = 400 kHz	-	-	300	μA
		Sleep patterns	-	0.2	1.0	μA
V_{IH}	Input high level	Digital pins (SCL, SDA, A2 to A0)	0.7 × V_{CC}	-	V_{CC} + 0.3	V
V_{IL}	Enter low level	Digital pins	−0.3	-	0.3 × V_{CC}	V
$V_{I(hys)}$	Enter the hysteresis voltage	SCL and SDA pins	-	300	-	mV
		A2, A1, A0 pins	-	150	-	mV
I_{IH}	High voltage input cu-rrent	Digital pin; VI = VCC	−1.0	-	+1.0	μA
I_{IL}	Low voltage input cur-rent	Digital pin; VI = 0 V	−1.0	-	+1.0	μA
V_{OL}	Output low voltage	SDA and OS pins; IOL = 3 mA	-	-	0.4	V
		I_{OL} = 4 mA	-	-	0.8	V
I_{LO}	Output leakage current	SDA and OS pins; VOH = VCC	-	-	10	μA
N_{fault}	Number of defects	Programmable; fault count co-nversion	1	-	6	
$T_{th(ots)}$	Overtemperature shutd-own threshold tempera-ture	Windows default	-	80	-	°C
T_{hys}	Recoil temperature po-int	Windows default	-	75	-	°C
C_i	Input capacitance	Digital pins	-	20	-	pF

[1] The typical value is obtained at V CC = 3.3 V and Tamb = 25 oC.

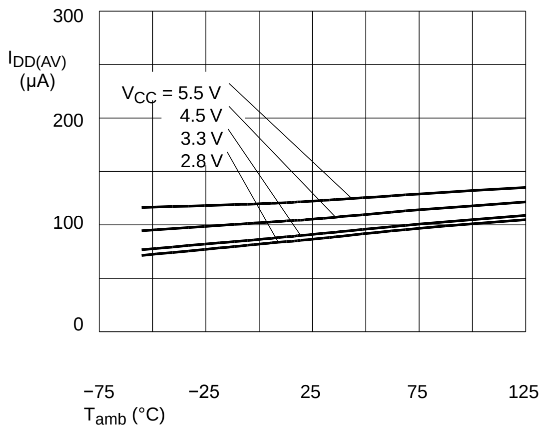


Table 14. Average current versus temperature curve when I2C is not activated

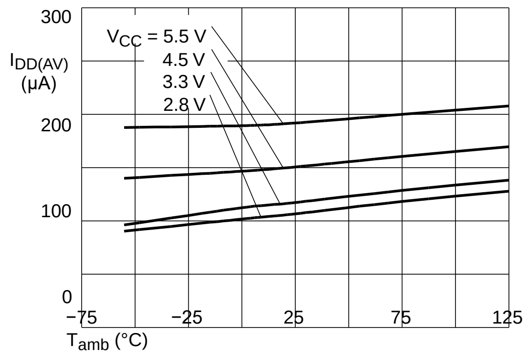


Table 15. Average current versus temperature curve when I2C is activated

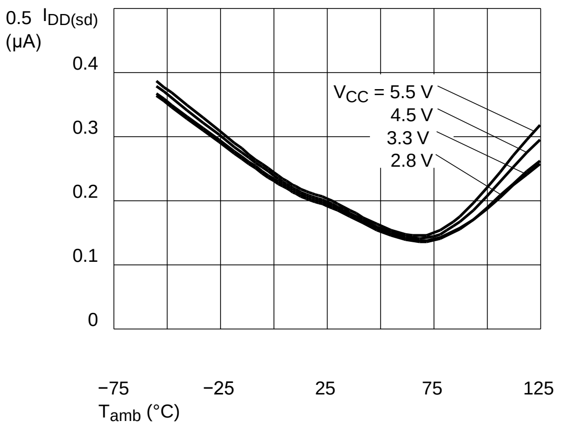


Table 16. Relationship between power supply current and temperature under sleep mode

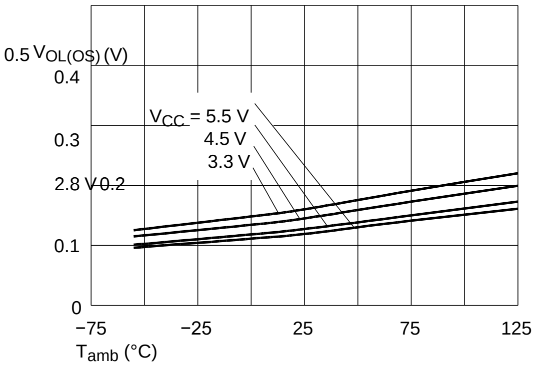


Table 17. Relationship between OS output voltage and temperature when IOL = 4 mA

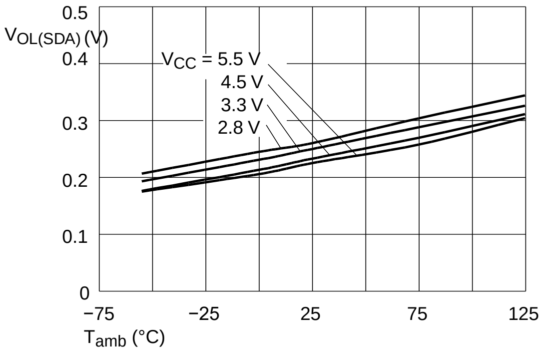


Table 18. Relationship between SDA voltage and temperature when IOL = 4 mA

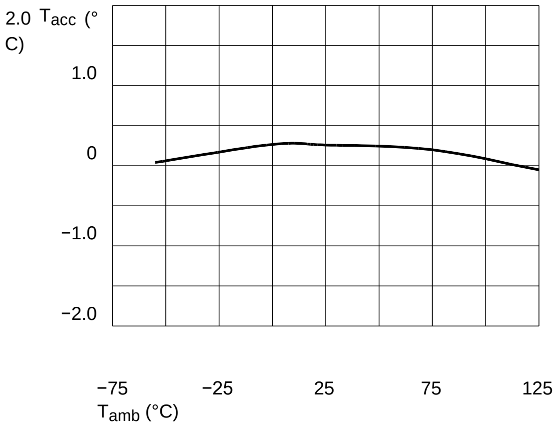


Fig 19. Typical temperature measurement accuracy when VCC = 3.3V

12. dynamic characteristis

Table 19. Dynamic characteristics of I2C bus interface ~~[1]~~

VCC = 2.8 V to 5.5 V; Tamb = ?55 ° C to +125 ° C; unless otherwise specified.

Symbol	Parameter	State	Minimum	Typical case	Maximum	Unit
f_{SCL}	SCL clock frequency	See Figure 20	0.02	-	400	kHz
t_{HIGH}	SCL clock high period		0.6	-	-	µs
t_{LOW}	SCL clock low level cycle		1.3	-	-	µs
$t_{HD;STA}$	Keep the start signal (repeat) for a certain period of time		100	-	-	ns
$t_{SU;DAT}$	Data build time		100	-	-	ns
$t_{HD;DAT}$	Data retention time		0	-	-	ns
$t_{SU;STO}$	Stop signal establishment time		100	-	-	ns
t_f	Drop-out time	SDA and OS output ports; C_L = 400 pF; I_{OL} = 3 mA	-	250	-	ns
t_{to}	Time-out	[2][3]	75	-	200	ms

[1] These specifications are guaranteed by design and are not tested in production.

[2] This is the lower time limit for SDA serial interface reset.

[3] Keeping the SDA line low for more than tto will cause the GX21M15 to reset the SDA to an idle state for serial bus communication (SDA is 1).

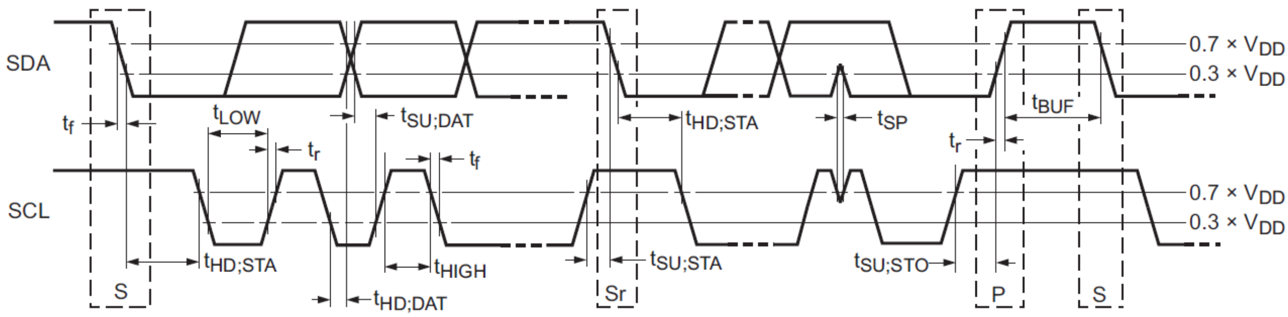
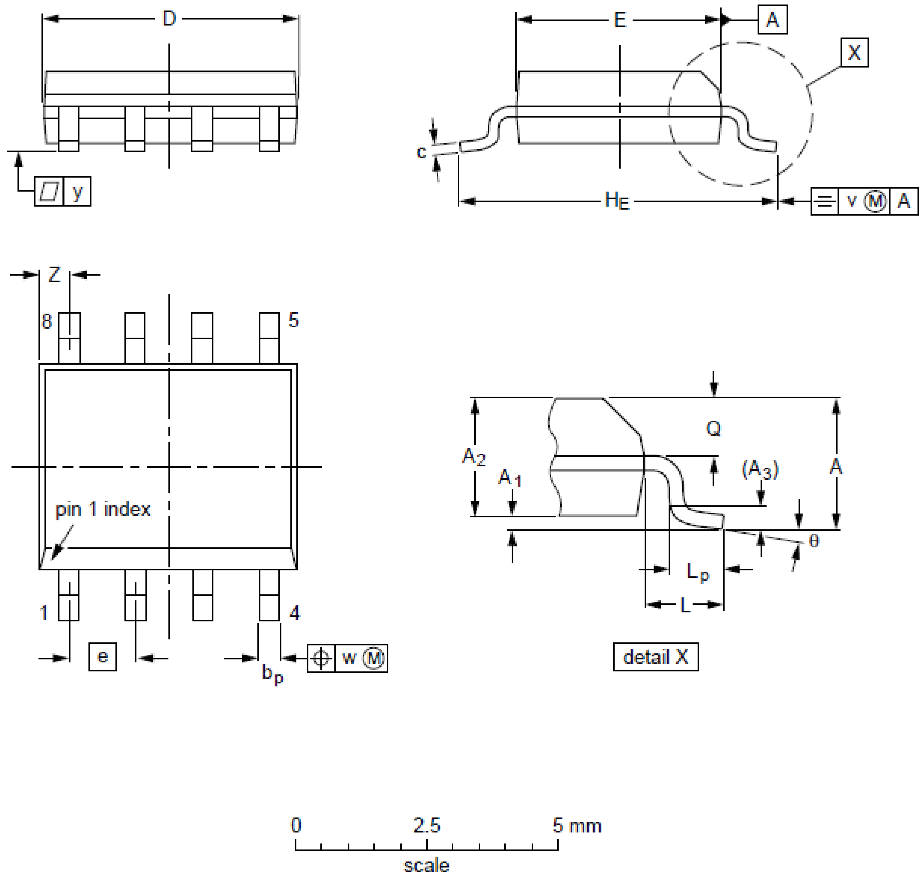


Figure 20. Time series diagram

13. Package information

SOP8: Small plastic package with dimensions: 8 lead plastic body width 3.9 mm



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

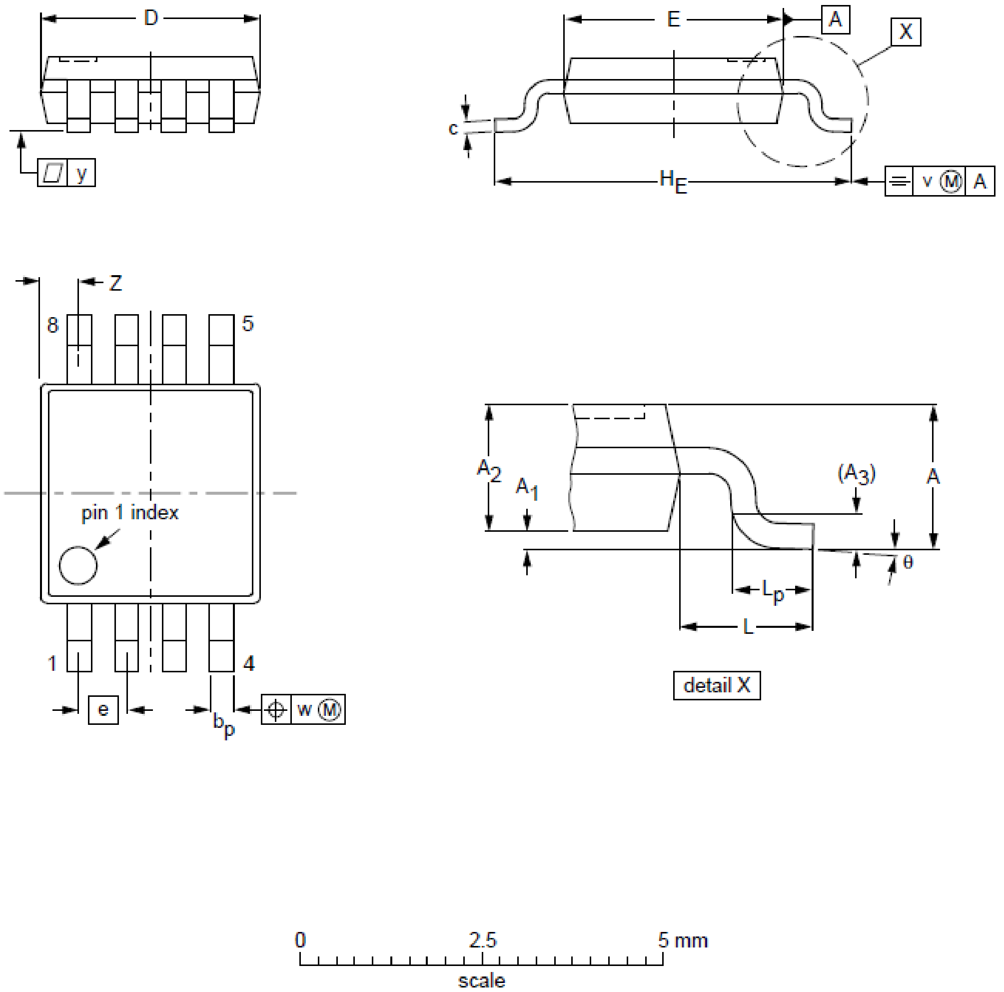
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

Figure 21. SOP8 package size diagram

MSOP8/TSSOP8: Thin plastic package with small size and shape: 8 leads, plastic body width 3 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

Figure 22. MSOP8/TSSOP8 package size diagram

14. Welding: PCB pin size diagram

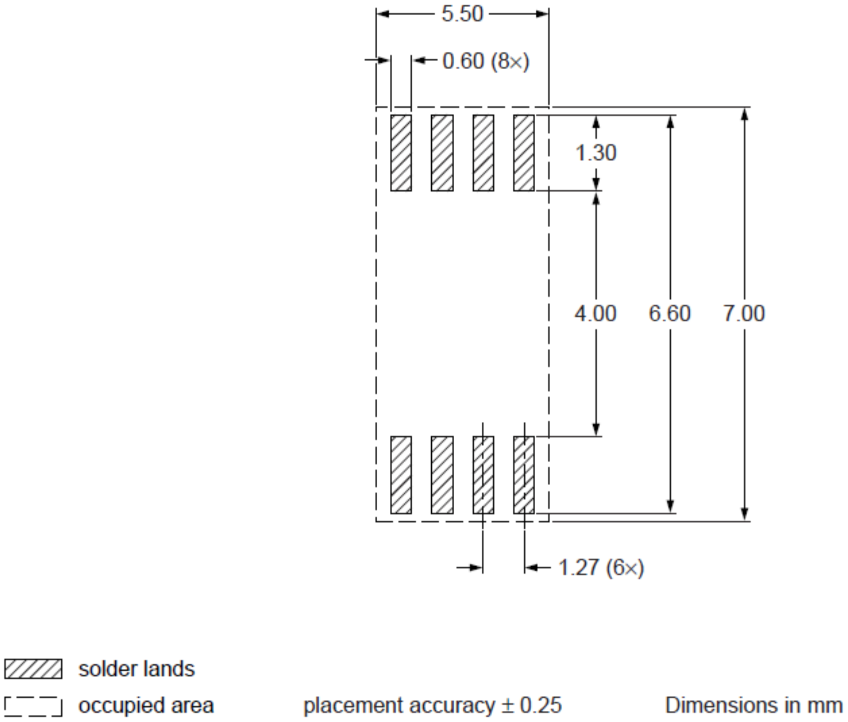


Figure 23. SOP8 PCB Pin size diagram

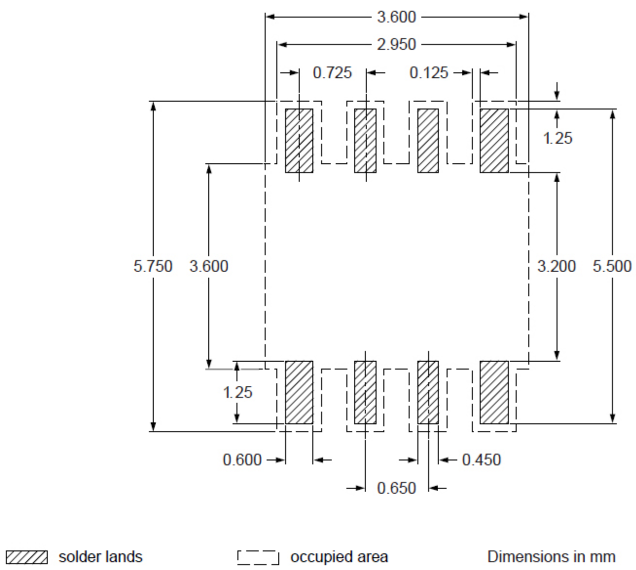
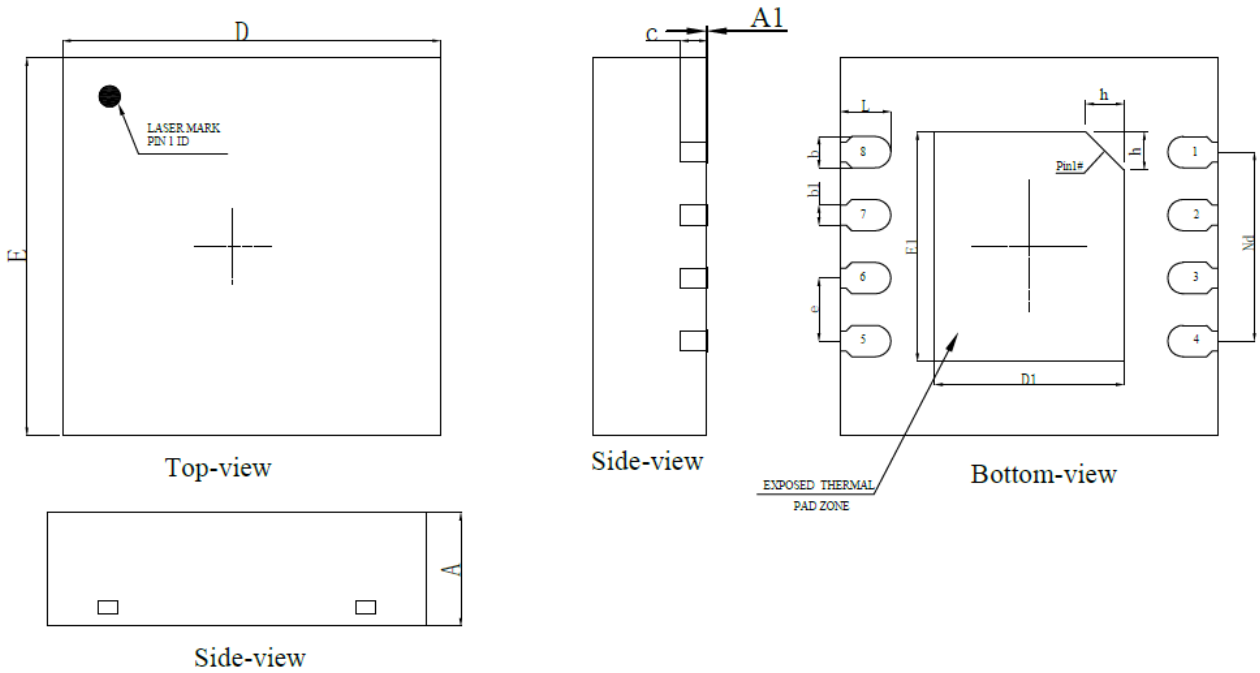


Figure 24. MSOP8/TSSOP8 PCB pin size

DFN8: Thin plastic package with reduced size and shape: 8 leads, plastic body width 3 mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.20	0.25	0.30
b1	0.20REF		
c	0.203REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.40	1.50	1.60
E1	1.75	1.85	1.95
e	0.50		
h	0.20	0.30	0.40
L	0.35	0.40	0.45
Nd	1.50		

15 Order information

Buy the code	Device	Package	Standard package quantity	Remarks
GX21M15-T&R	GX21M15	SOP8	4000	Tape and reel
GX21M15U-T&R	GX21M15U	MSOP8	4000	Tape and reel
GX21M15D-T&R	GX21M15D	DFN8	4000	Tape and reel