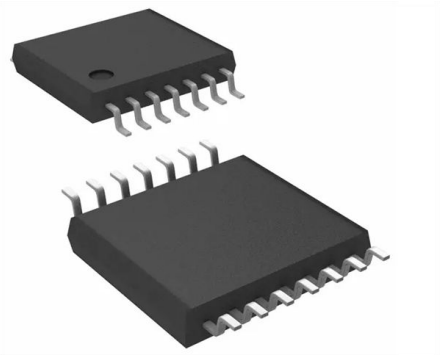
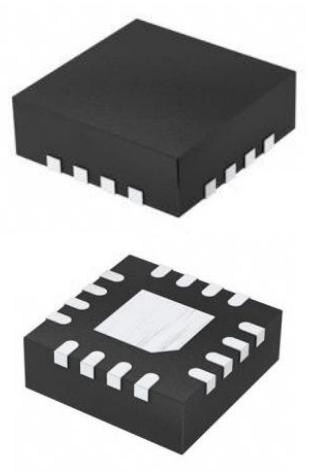
96kHz 24 position ΔΣ ADC

MS1808 is a stereo A/D converter with sampling rates of 8kHz to 96kHz, suitable for professional audio systems for consumers.

MS1808 Achieves its high precision through the use of enhanced dual-bit ΔΣ technology. MS1808 It is a single-ended analog input, so no external components are required. There are two types of audio interfaces (most significant bit aligned, I 2 S) suitable for systems like DTV, DVR, and AV receivers.



TSSOP14



QFN16

main features

- Linear phase anti-aliasing digital filter
- single-ended input
- A digital high-pass filter with offset voltage elimination
- Signal-to-noise distortion ratio: 85dB
- dynamic range: 95dB
- noise-signal ratio: 95dB
- sampling rate 8kHz to 96kHz
- master clock:
  256fs/384fs/512fs/768fs (8kHz ~ 48kHz)
  256fs/384fs (48kHz ~ 96kHz)
- Master/slave mode
- Audio interface: 24-bit most significant bit aligned /I 2 S
- Power supply: 4.5 ~ 5.5V analog, 2.7 ~ 5.5V digital
- Temperature range-20 ~ 85
- TSSOP 14, QFN16 packaging

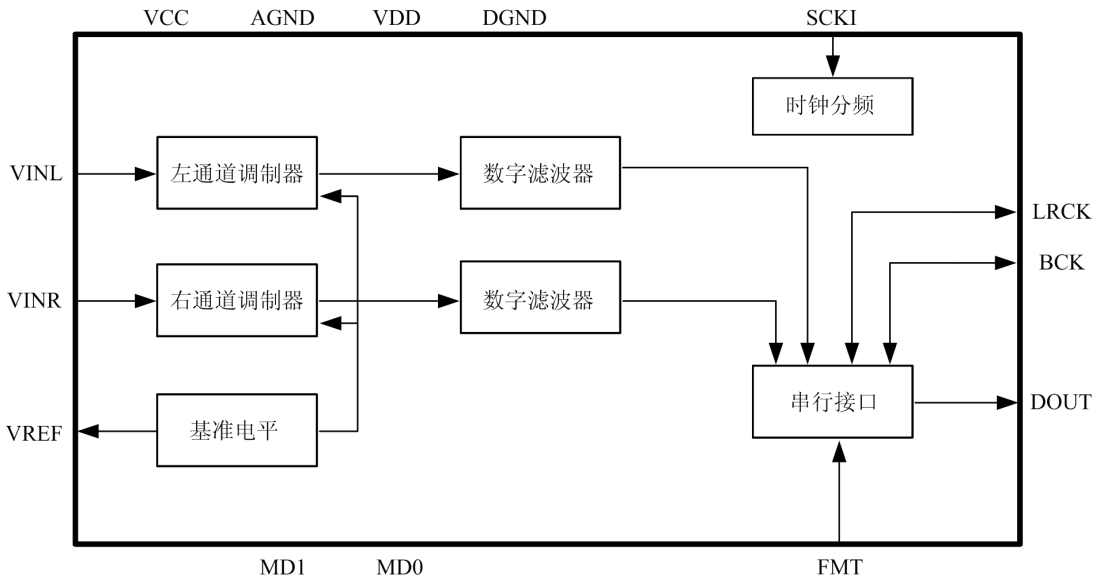
Product specification classification

Product	Packaging form	Print the name
MS1808	TSSOP14	MS1808
MS1808	QFN16	MS1808N

apply

- DVD, recorder
- figure TV
- CD recorder

Internal block diagram



absolute rating

AGND, DGND = 0V (1)

Parameter		Symbol	Parameter range	Unit
Service voltage	Imitate Number | AGND-DGND | (2)	VCC VDD ΔGND	-0.3 ~ 6.0 -0.3 ~ 6.0 0.3	V V V
Any input current to a pin except the power supply		IIN	±10	mA
Simulate input voltage (VINL, VINR pins)		VINA	-0.3 ~ VCC+0.3	V
Digital input voltage (3)		VIND	-0.3 ~ VDD+0.3	V
Ambient temperature		Ta	-20 ~ 85	℃
Storage temperature		Tstg	-65 ~ 150	℃

1. All voltages are based on the ground
2. AGND and DGND must be connected to the same analog ground
3. FMT, SCKI, BCK, LRCK, MD1, MD0 pins

Warning: Operation above these limits may cause permanent damage to the device. Normal operation is not guaranteed under these extreme conditions.

Recommend working voltage

AGND，DGND = 0V

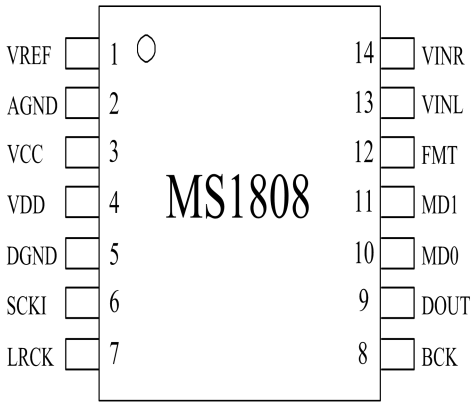
Parameter		Symbol	Parameter range	Unit
Supply voltage (4)	Imitate Figure	VCC VDD	4.5 ~ 5.5 2.7 ~ VCC	V V

4. There is no explicit requirement for the order in which VCC and VDD are powered on

Useless pin handling

Class	Name of the tube or foot	Set up
Imitate	VINR	The pins should be open
	VINL	The pins should be open

Pin layout



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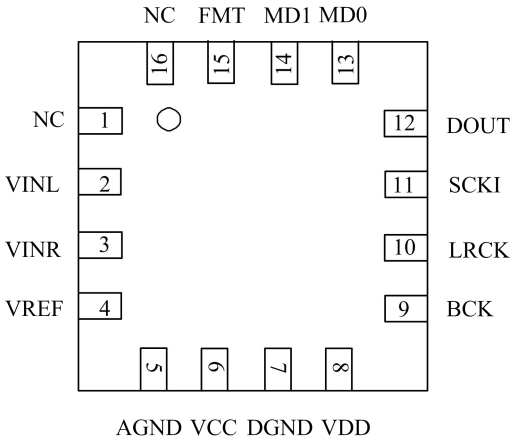


QFN16

Pin description

Pin number	Name of the tube or foot	I/O	Description of the tubes and feet
TSSOP14 Packaging			
1	VREF	O	Common-mode voltage output pin, VCC/2 ADC input bias voltage
2	AGND	-	Simulate the ground pin
3	VCC	-	Simulate power supply pin, 4.5 ~ 5.5V
4	VDD	-	Digital power pin, 2.7 ~ 5.5V
5	DGND	-	Digital ground pin
6	SCKI	I	Main clock input pin
7	LRCK	I/O	Output channel clock pin
8	BCK	I/O	Audio serial port data clock pin

9	DOUT	O	Audio serial port data output pin
10	MD0	I	Mode selection 0 pin
11	MD1	I	Mode selection 1 pin
12	FMT	I	Select the pin for the audio interface type "L": 24-bit compatible with I2 S, "H": 24-bit most significant bit aligned
13	VINL	I	Lch simulates the input pin
14	VINR	I	The Rch simulates the input pin
QFN16 Packaging			
1	NC		Connectionless
2	VINL	I	Lch simulates input pins
3	VINR	I	Rch Simulate input pins
4	VREF	O	Common-mode voltage output pin, VCC/2 ADC input bias voltage
5	AGND	-	Simulate the ground pin
6	VCC	-	Simulate power supply pin, 4.5 ~ 5.5V
7	DGND	-	Digital ground pin
8	VDD	-	Digital power pin, 2.7 ~ 5.5V
9	BCK	I/O	Audio serial port data clock pin
10	LRCK	I/O	Output channel clock pin
11	SCKI	I	Main clock input pin
12	DOUT	O	Audio serial port data output pin
13	MD0	I	Mode selection 0 pin
14	MD1	I	Mode selection 1 pin
15	FMT	I	Select the pin for the audio interface type "L": 24-bit compatible with I2 S, "H": 24-bit most significant bit aligned
16	NC		Connectionless

Electrical parameters

Simulation features

Unless otherwise specified, Ta = 25 ; VCC = 5.0V, VDD = 3.3V; AGND = DGND = 0V; fs = 48kHz, 96kHz; BCK = 64fs; signal frequency = 1kHz; 24-bit data; the measured frequency is 20Hz ~ 20kHz at fs=48kHz and 40Hz ~ 40kHz at fs = 96kHz

Parameter			Minimum	Typical case	Maximum	Unit
The ADC simulates the input characteristics						
Accuracy					24	Bits
Input voltage (5)			2.7	3.0	3.3	Vpp
Signal-to-noise distortion ratio	fs = 48kHz BW = 20kHz	-1dBFS	75	85		dB
		-60dBFS		39		dB
	fs = 96kHz BW = 40kHz	-1dBFS		90		dB
		-60dBFS		38		dB
Dynamic range (-60dBFS, A-weighted)			85	95		dB
Signal-to-noise ratio (A-weighted)			85	95		dB
Input impedence	fs = 48kHz		13	20		kΩ
	fs = 96kHz		9	14		kΩ
Internal access is isolated			80	85		dB
Internal channel gain mismatch				0.1	0.5	dB
Gain drift				100	-	ppm/℃
Power suppression ratio (6)			-	50		dB
Power Supply Voltage						
Normal operation of supply current VCC VDD (fs = 48kHz) VDD (fs = 96kHz)				 10 2 4	 16 5 9	 mA mA mA

5. This value is the full swing of the input voltage (0dB), which is proportional to the input voltage VCC. Vin=0.6 * VCC (Vpp)
6. In the power suppression ratio, the power supply is VCC and VDD with 1kHz and 50mVpp AC signals

Filter characteristics fs = 48kHz

Ta = -20℃ ~ 85℃； VCC = 4.5V ~ 5.5V； VDD = 2.7V ~ 5.5V

Parameter		Signal	Minimum	Typical case	Maximum	Unit
ADC digital filter (extracting low-pass filter)						
Passband (7)	±0.1dB -0.2dB -3.0dB	PB	0 - -	20.0 23.0	18.9 - -	kHz kHz kHz
Stop band		SB	28			kHz
Passband ripple		PR			±0.04	dB
Band-stop attenuation		SA	68			dB
Group delay distortion		ΔGD		0		us
Group delay		GD		16		1/fs
ADC digital filter (high pass filter)						
Frequency respo-nse (8)	-3dB -0.1dB	FR		1.0 6.5		Hz Hz

Filter characteristics fs = 96kHz

Ta = -20℃ ~ 85℃； VCC = 4.5V ~ 5.5V； VDD = 2.7V ~ 5.5V

Parameter		Signal	Minimum	Typical case	Maximum	Unit
ADC digital filter (extracting low-pass filter)						
Passband (7)	±0.1dB -0.2dB -3.0dB	PB	0 - -	40.0 46.0	37.8 -	kHz kHz kHz
Stop band		SB	56			kHz
Passband ripple		PR			±0.04	dB
Band-stop attenuation		SA	68			dB
Group delay distortion		ΔGD		0		us
Group delay		GD		16		1/fs
ADC digital filter (high pass filter)						
Frequency respo-nse (8)	-3dB -0.1dB	FR		2.0 13.0		Hz Hz

7. The passband and stopband frequencies change with fs, such as: PB=18.9kHz@±0.1dB is 0.39375*fs
8. The computational delay time introduced by digital filtering

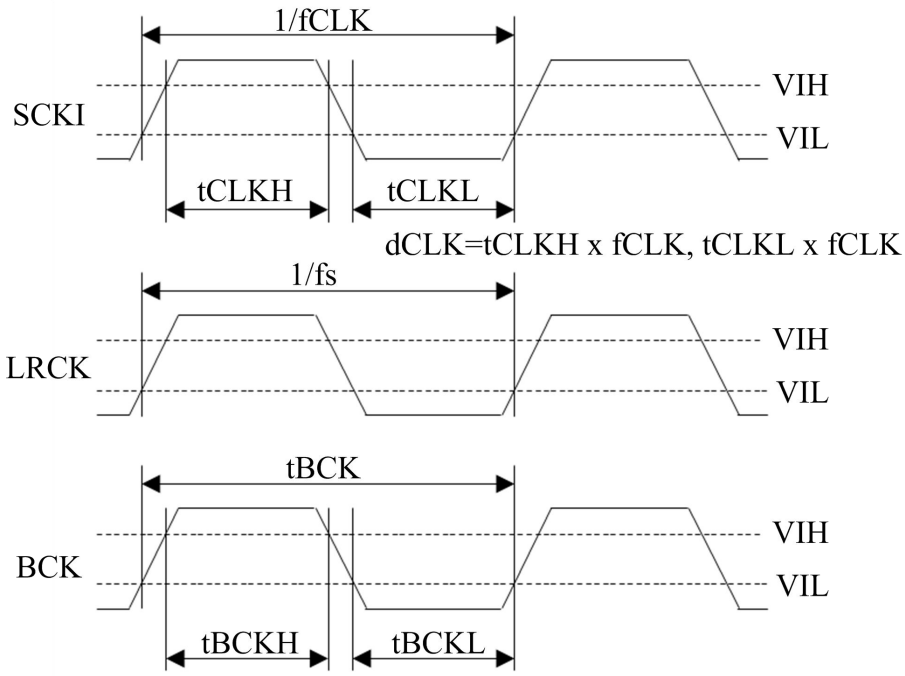
switching characteristic

Ta = -20℃ ~ 85℃； VCC = 4.5V ~ 5.5V； VDD = 2.7V ~ 5.5V； CL=20pF

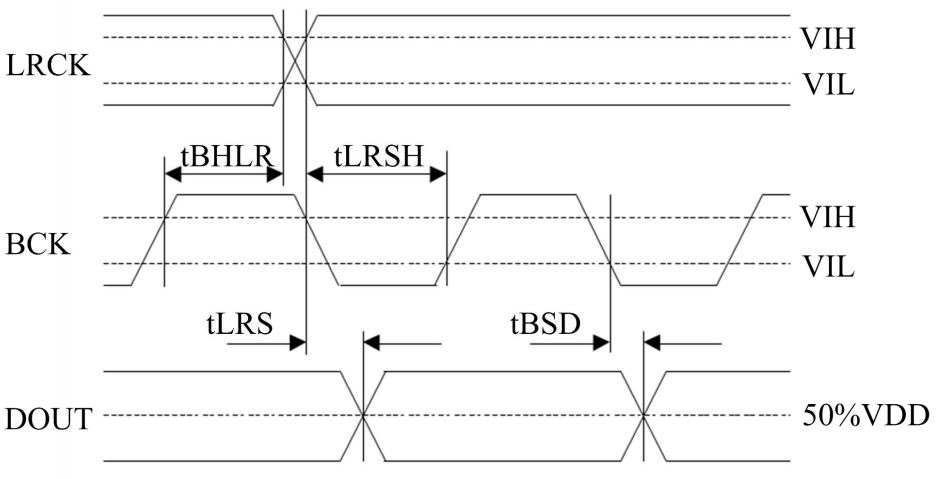
Parameter	Signal	Minimum	Typical case	Maximum	Unit
Main clock time 512fs, 256fs frequency duty cycle 768fs, 384fs frequency duty cycle	fCLK dCLK fCLK dCLK	2.048 40 3.072 40		24.576 60 36.864 60	MHz % MHz%
LRCK frequency Duty cycle from machine mode Host mode	fs	8 45	 50	96 55	kHz % %
Audio interface time **From the machine mode** BCK period BCK Low pulse width High pulse width LRCK edge to BCK " " (9) BCK " " to LRCK edge (9) LRCK to DOUT(MSB) (except I2S mode) BCK " " to DOUT **Host mode** BCK frequency BCK, duty cycle BCK " " to LRCK BCK " " to DOUT	 tBCK tBCKL tBCKH tLRSH tBHLR tLRS tBSD fBCK dBCK tMBLR tBSD	 160 65 65 30 30 -20 -20	 64fs 50	 35 35 20 35	 ns ns ns ns ns ns ns Hz % ns ns

9. The rising edge of BCK must not be on the rising and falling edges of LRCK

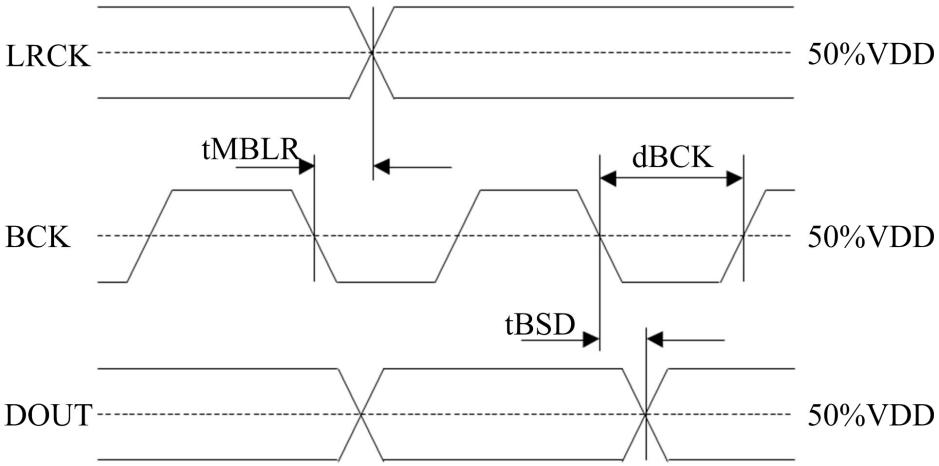
sequence chart



Clock timing



Audio interface timing (slave mode)



Audio interface timing (host mode)

Operation overview

hardware control

The pull-up and pull-down resistors and the GPIO of the digital IC are selected by the output encoding format and operating mode through the FMT, MD0, and MD1 pins of the control chip.

AT system clock

MS1808 Supports 256fs, 384fs, and 512fs as system clock. fs is the audio sampling frequency, and the input pin of the system clock is SCKI.

Table 1 shows the relationship between some typical sampling frequencies and system clock frequencies.

fs	SCKI		
	256fs	384fs	512fs
32kHz	8.192MHz	12.288 MHz	16.384 MHz
44.1kHz	11.2896 MHz	16.9344 MHz	22.5792 MHz
48 kHz	12.288 MHz	18.432 MHz	24.576 MHz
96 kHz	24.576 MHz	36.864 MHz	N/A

Table 1: Examples of system clocks

Interface mode

MD1 and MD0 are used as mode selection pins to select host mode and slave mode. Table 2 shows the interface mode selection.

In host mode, BCK and LRCK are used as output pins with a frequency of 64fs for BCK.

In slave mode, BCK and LRCK are input pins with BCK frequency of 48fs or 64fs.

MD1	MD0	Interface mode
0	0	From machine mode (256fs, 384fs, 512fs automatic detection)
0	1	Host mode (512fs)
1	0	Host mode (384fs)
1	1	Host mode (256fs)

Table 2: Interface mode

data format

Mode	FMT	Data format
0	L	24bit, I^2S Compatible
	H	MSB
1		24bit, justified

Table 3: Data format

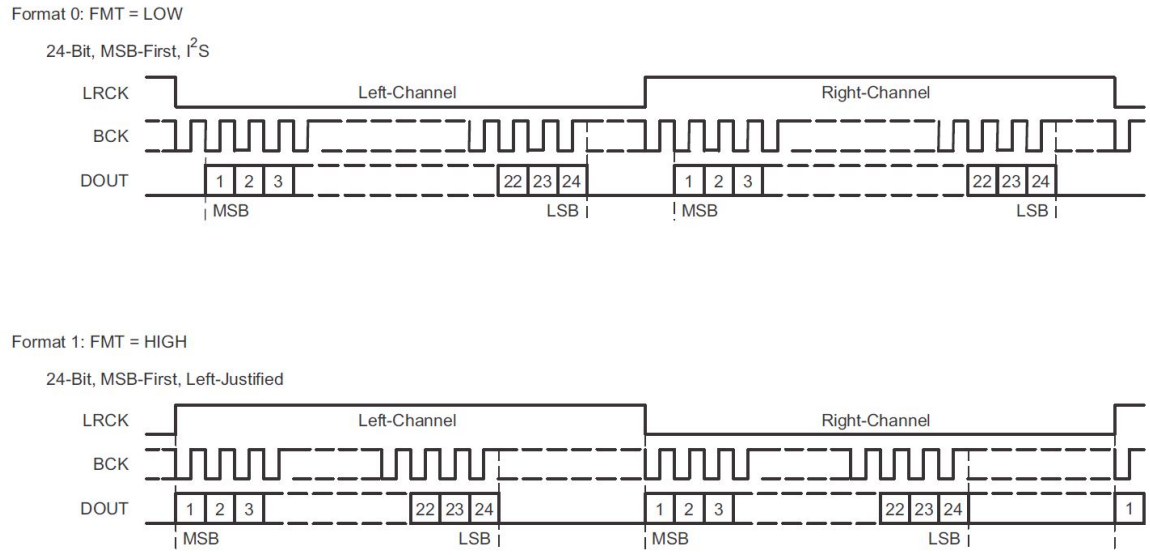


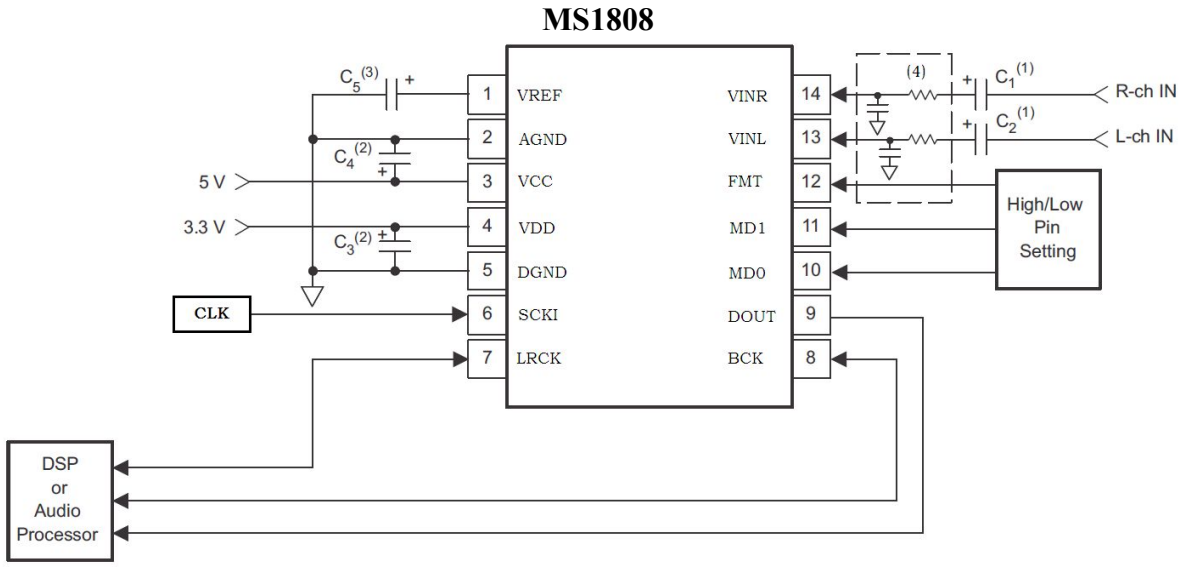
Figure 1: Audio data format

Digital high-pass filter

The ADC has a digital high-pass filter to eliminate DC distortion. The cutoff point of the high-pass filter is 1.0Hz (@fs = 48kHz) and extends with its sampling frequency (fs).

During initialization, the ADC digital data output of both channels is set to the binary complement "0". After initialization, the ADC output gradually corresponds to the input signal (it takes about group delay time to stabilize).

Typical application



1. C1, C2: 10uF AC coupling capacitor
2. C3, C4: 10uF electrolytic capacitors and 0.1uF ceramic capacitors
3. C5:2.2uF Capacitors
4. Optional external anti-aliasing filter

Decoupling of ground and power supply

MS1808 requires special attention to the layout of power and ground. Additionally, if VCC and VDD are separated, their power-up sequence is not critical. The AGND and DGND of the MS1808 must be connected to the same analog ground. The system's analog ground and digital ground should be connected together and close to the power supply of the printed circuit board. The decoupling capacitor should be as close as possible to the MS 1808, with small ceramic capacitors being placed nearest.

Power base

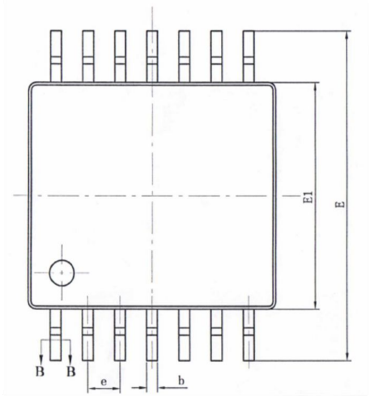
The range of the simulated voltage input is set by VCC, and VREF is 50% of VCC. A 2.2uF capacitor is attached to the VREF pin. To avoid unwanted coupling into the MS1808, all signals, especially the clock, should be kept away from the VREF pin.

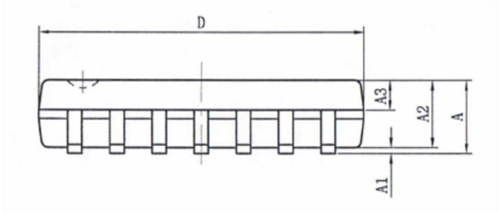
analog input

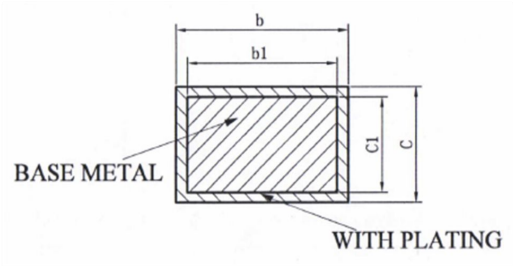
The ADC input is single-ended and internally biased through a 20kΩ resistor to the common-mode voltage (50% * VCC) (typical @fs=48kHz). The input signal range expands with the power supply voltage, typically 0.6 * VCC Vpp (typical). The ADC output data format is binary two's complement. An internal high-pass filter eliminates DC offset voltages.

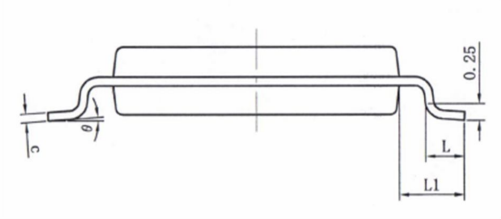
Encapsulate the shape diagram

TSSOP14



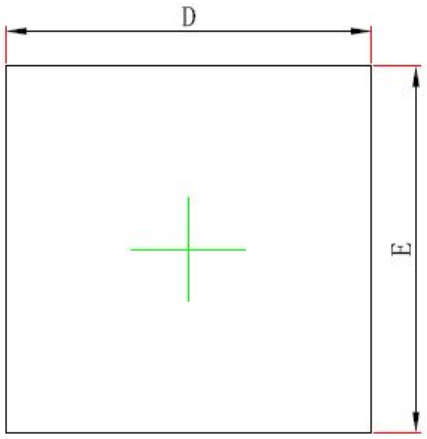




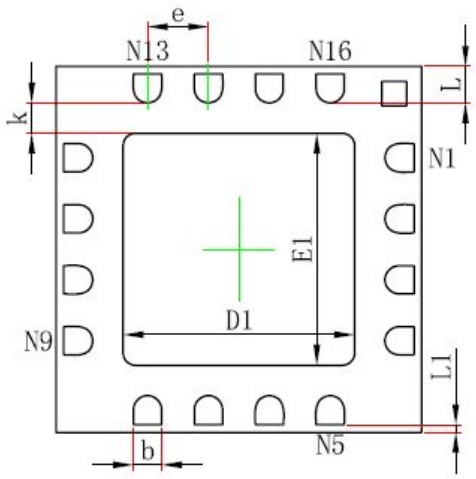


Symbol	Size (mm)		
	Minimum	Typical case	Maximum
A			1.20
A1	0.05		0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20		0.30
b1	0.19	0.22	0.25
c	0.13		0.19
c1	0.12	0.13	0.14
D	4.86	4.96	5.06
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45		0.75
L1	1.00BSC		
θ	0		8°
L/F Carrier size (mil)	79×79	90×110	
	118×153		

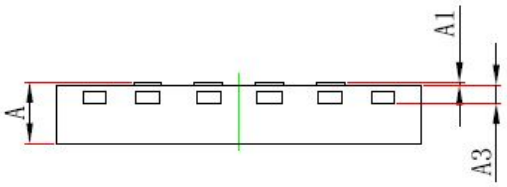
QFN16



Top View



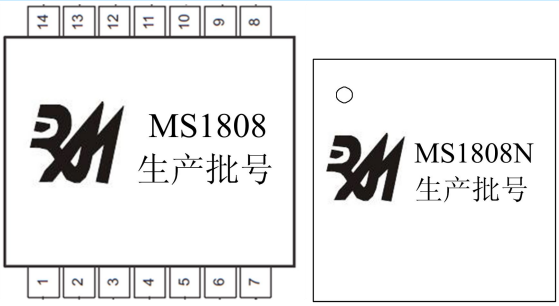
Bottom View



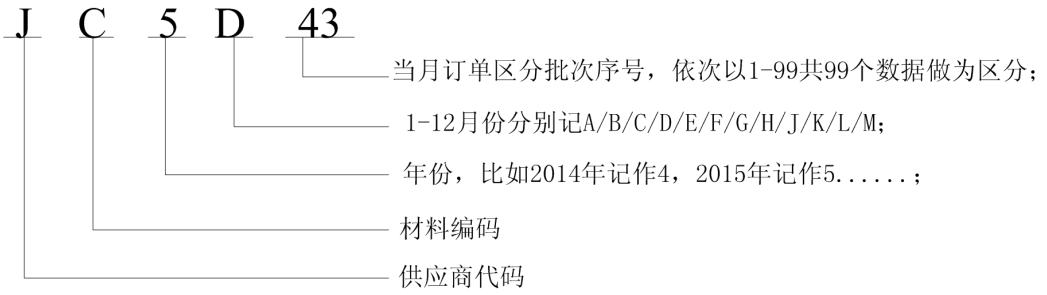
Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450/0.500/0.550	0.550/0.600/0.650	0.018/0.020/0.022	0.022/0.024/0.026
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	1.800	2.000	0.071	0.079
E1	1.800	2.000	0.071	0.079
k	0.200MIN.		0.008MIN.	
b	0.230	0.330	0.009	0.013
e	0.500TYP.		0.020TYP.	
L	0.250	0.350	0.010	0.014
L1	0.013	0.113	0.000	0.004

Stamp specifications



I. Introduction of Seal content MS1808/MS1808N: Product model production batch number:
Example: JC5D43



2. Standard requirements for seals

Laser printing is used, the whole is centered and the Arial font is used.

3. Packaging specifications

Model	One / plate	Plates/cans	1 / box	Box/case	1 / box
MS1808	3000	1	3000	8	24000
MS1808N	3000	1	3000	8	24000

MOS circuit operation precautions:

Static electricity can be generated in many places. The following precautions can effectively prevent the damage of MOS circuit caused by static discharge:

- The operator should be grounded through the anti-static wristband.
- The equipment housing must be grounded.
- Tools used in assembly must be grounded.
- Conductive packaging or anti-static material packaging or transportation must be used.