Four-channel differential line driver

Chip description

GC26L32S is a low-voltage 5V four-channel differential line receiving chip that can receive differential balanced and unbalanced digital data. The enable control terminal can simultaneously control the four channels of reception, where G is valid at high level and GN is valid at low level. When the input is open, the output is high level.

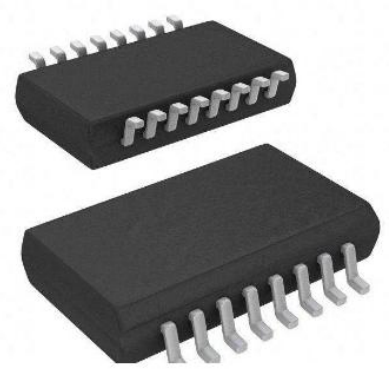
GC26L32S Use SOP16 packaging.

Chip application

- Automotive applications
- factory automation
- ATMs and banknote counters
- AC and servo motor drive

Chip features

- Complies with ANSI TIA/EIA-422-B and ITU V1.0 and V1.11 requirements
- Common input range: ±7V
- Input sensitivity: positive and negative 200mV
- Input hysteresis: 50mV
- 5V single power supply
- Low power Schottky circuit
- three-state output
- Complementary enables input control
- Minimum 12KΩ input impedance

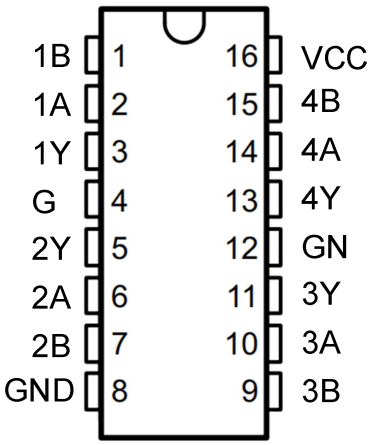


Product name	Package	Description
GC26L32S	SOP816	10*3. 9mm e=1.27

Packaging instructions

Per plate	Per box	Per case
4K	8K	64K

Pin distribution diagram



SOP16

Pin description

Pin number	Name of the tube	I/O	Description of the tubes and feet
1	1B	I	First channel receiver B input
2	1A	I	First channel receiver A input
3	1Z	O	First channel receiver output
4	G	I	Enable control (high level active)
5	2Y	O	Output of the second channel receiver
6	2A	I	Second channel receiver A input
7	2B	I	Second channel receiver B input
8	GND	--	The earth
9	3B	I	Third channel receiver B input
10	3A	I	Third channel receiver A input
11	3Z	O	Output of third channel receiver
12	GN	I	Reverse enable control (low level active)
13	4Y	O	Fourth channel receiver output
14	4A	I	Fourth channel receiver A input
15	4B	I	Fourth channel receiver B input
16	VCC	--	Source

Internal block diagram

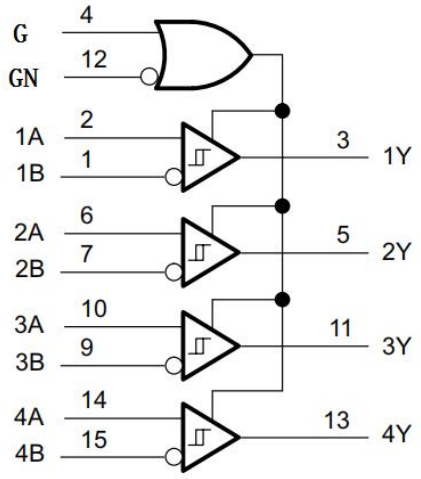


Figure 1 GC26L32S Internal block diagram

Extreme parameters (T = 25 in general without other special notes)

Parameter	Symbol	Parameter range	Unit
Working voltage	VCC	-0.3~7	V
Differential terminal input voltage range		±25	V
Control the input voltage range			
Working temperature	Top	-40~100	℃
Junction temperature	Tjmax	-40~150	℃
Storage temperature	Tstg	-60~150	℃
Electrostatic protection (human body mode)	ESD	±1000	V

Recommended working environment:(no other description, T=25)

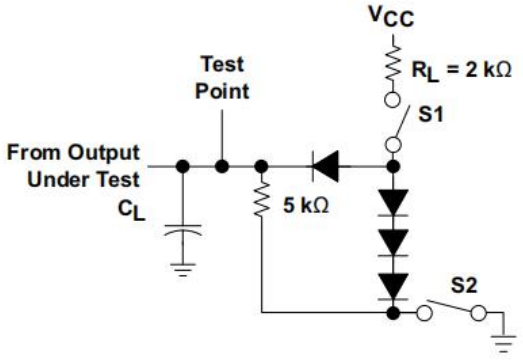
Parameter	Symbol	Test condition	Least value	Representative value	Crest value	Unit
Source	VCC		4.75	5	5.25	V
Input high level	VIH		2			V
Enter low level	VIL				0.8	V
Common-mode input voltage	VIC				±7	V
High level output current	IOH				-440	uA
Low level output current	IOL				+8	mA
Working temperature	T_a		-40		100	℃

Electrical parameters (T=25 , VCC=5V in general without other special notes)

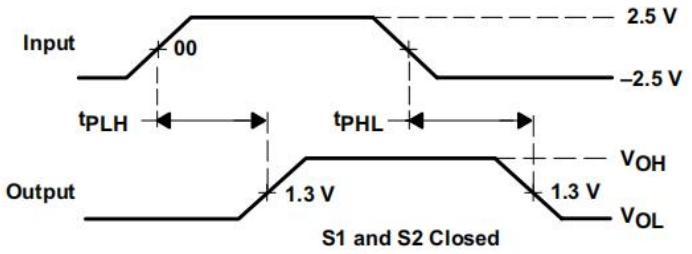
Parameter	Symbol	Test condition	Least value	Representative value	Crest value	Unit
The rising edge is input threshold voltage	VIT+	VO = 2V, IOH =–440 uA			0.2	V
The voltage threshold is decreased along the input	VIT+	VO = 0.45V, IOL =8mA	-0.2			V
Input hysteresis voltage	Vhys			50		mV
Enable the input clamp voltage	VIK	VCC=4.75V, II=-18mA			-1.5	V
High level output voltage	VOH	VCC=4.75V, VID=1V, VI（G)=0.8V, IOH=-440uA	2.5			V
Low level output voltage	VOL	VCC=4.75V, VID=-1V, VI（G)=0.8V			0.5	V
Three state output current	IOZ	VCC=5.25V, VO=2.4V			20	uA
		VCC=5.25V, VO=0.4V			-20	uA
Line input current	II	VI = 15V, other inputs from -10V to 15V			1.2	mA
		VI= -15V, other inputs from -15V to 10V			-1.7	mA
Enable high level input current	IIH	VI = 2.7V			20	uA
Enable low level input current	IIL	VI =			-0.36	mA

		0 .4 V				
Input resistance	ri	VIC= -15V to 15V, other input AC to ground	12	15		K Ω
Output short circuit current	Ios	VCC= 5.25 V	-15		-85	mA
Source current	Icc	Turn off the output		52	70	mA
Switching characteristic						
Low level to high level transmission delay	tPLH			27	50	ns
High level to low level transmission delay	tPHL			20	50	ns
Output to high level enable time	tPZH			30	45	ns
Output to low level enable time	tPZL			37	50	ns
Output high level turn-off time	tPHZ			35	45	ns
Output from low level turn-off time	tPLZ			32	40	ns

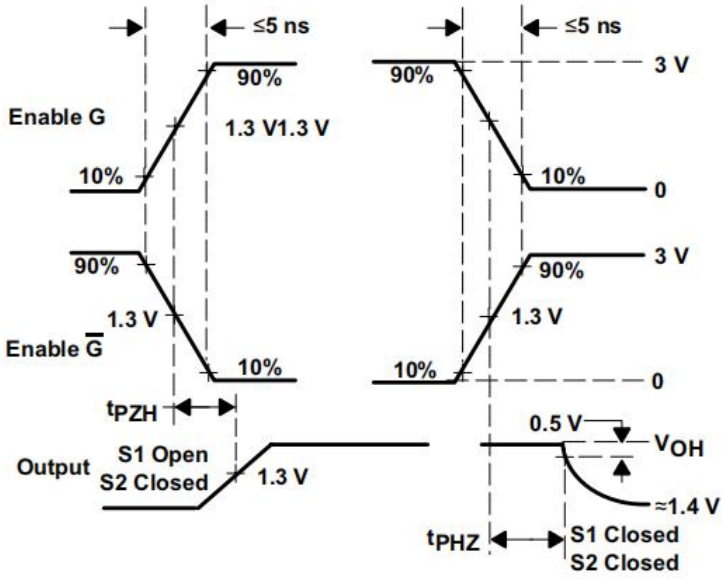
test circuit



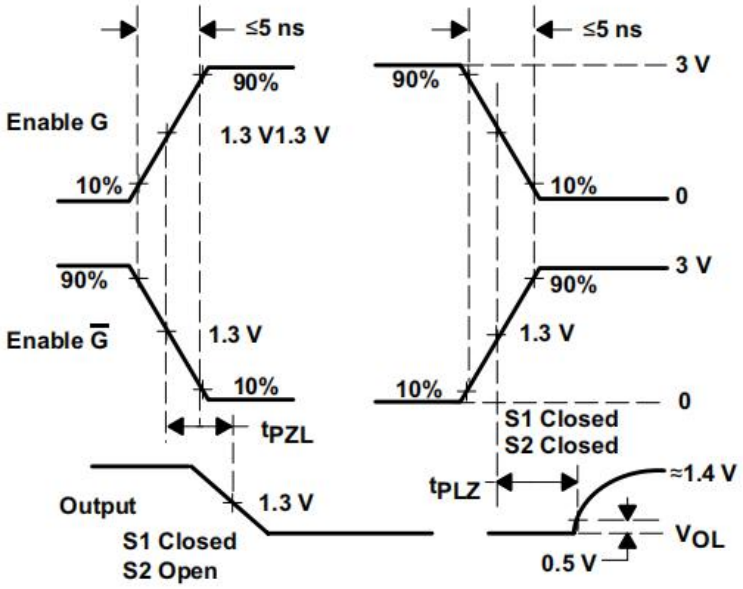
test circuit



tPLH and tPHL test waveforms



tPHZ and tPZH test waveforms



tPLZ and tPZL, test waveform

functional description

GC26L32S The differential bus receiver chip is a monolithic integrated circuit designed for one-way data communication and transmission

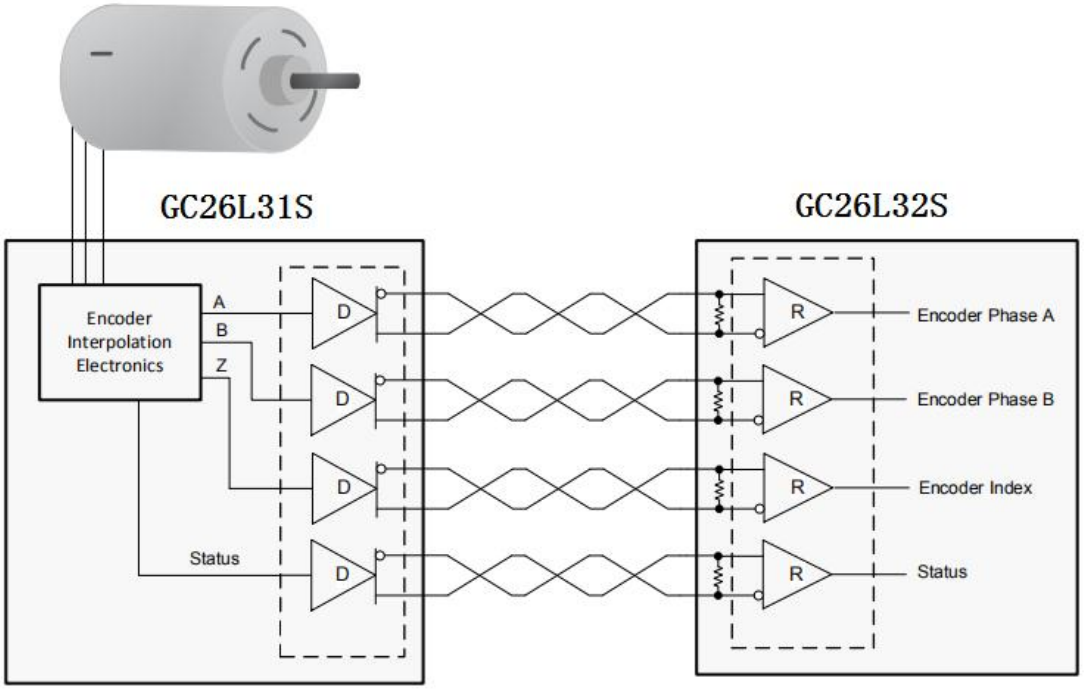
ANSI standard EIA/TIA-422-B and ITU, recommended V.11. It features four tri-state differential line receivers that can operate on a single 5-volt power supply. This device allows low-power or low-voltage MCUs to connect heavy machinery, subsystems, and other equipment over long wires up to 1000 meters, providing reliable and easy-to-use connections for any design.

Enable control

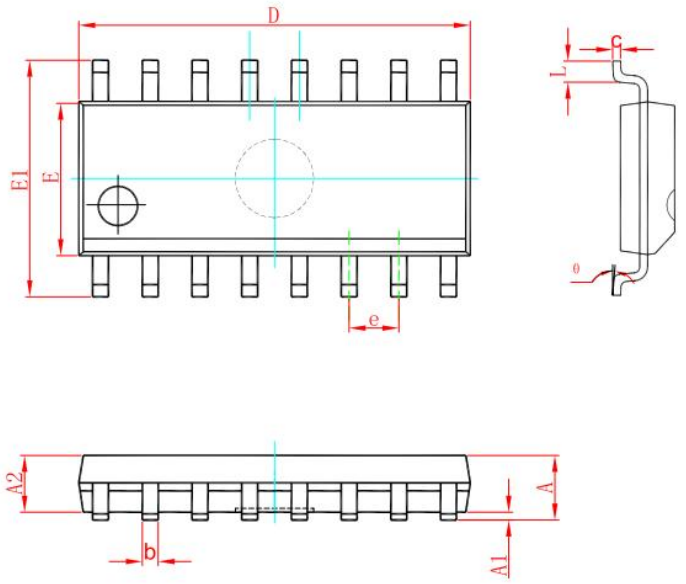
GC26L32S It is controlled by the G and GN input interfaces, and its control truth table is as follows:

Differential input A-B	Enable		Output
	G	GN	Y
VID ≥ VIT+	H	X	H
	X	L	H
VIT– ≤ VID ≤ VIT+	H	X	?
	X	L	?
VID ≤ VIT–	H	X	L
	X	L	L
X	L	H	Z
Open a way	H	X	H
	X	L	H

Typical application circuit diagram



SOP16 **UNIT: mm**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°