description

AT8313 Provides three independently controllable half-H bridge drivers, each capable of delivering a peak current of 2.5A or an RMS (root mean square) current of 1.75A. These can drive a three-phase brushless DC motor or other inductive loads such as solenoids. Each half-H bridge output stage consists of two N-type power MOSFET, with their ground terminals available for external detection of the output current value using a galvanometer resistor.

AT8313 Provides a universal comparator that can be used to limit the output current.

The internal shutdown function includes overcurrent protection, short circuit protection, undervoltage lockout protection and overtemperature protection, and provides a fault detection output pin.

AT8313 Two types of surface mount packages are provided, both with exposed heat dissipation pads, which can effectively improve the heat dissipation performance. One is QFN36 (6mm x 6mm) and the other is ETSSOP28

(9.7mm x 4.4mm). Both packages are lead-free and meet environmental standards.

apply

- HVAC any power-generating or power-driven machine
- Consumer products
- business automation equipment
- factory automation
- robot

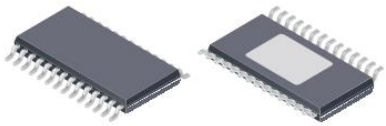
Model selection

Order number	Package	Pack
AT8313QNR	QFN6*6-36	Strips, 3000 beads per disc
AT8313QNR-H	QFN6*6-36	Strips, 3000 beads per disc
AT8313TPN	ETSSOP28	Strips, 3000 beads per disc

characteristic

Three and a half H-bridge motor drivers
Drive three-phase brushless DC motor (BL-DC)
Independent half-bridge control
Three independent grounding pins for current detection
Low RDS (ON) resistance, 0.45Ω (HS + LS)
2.5A drive output
Wide voltage supply, 8V-35V
A universal comparator is used to limit the flow
Built-in 3.3V 10mA reference voltage output
Over temperature protection
short-circuit protection
Under-voltage lockout protection

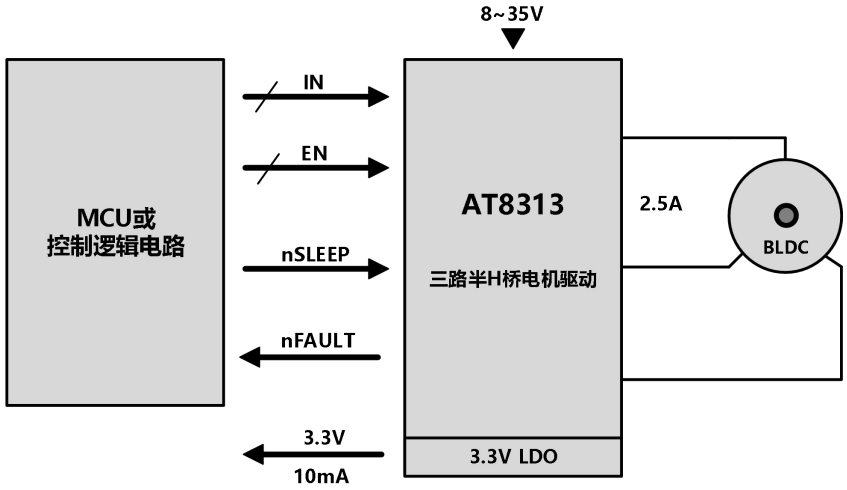
Packaging form



ETSSOP28

QFN36

Typical application schematic

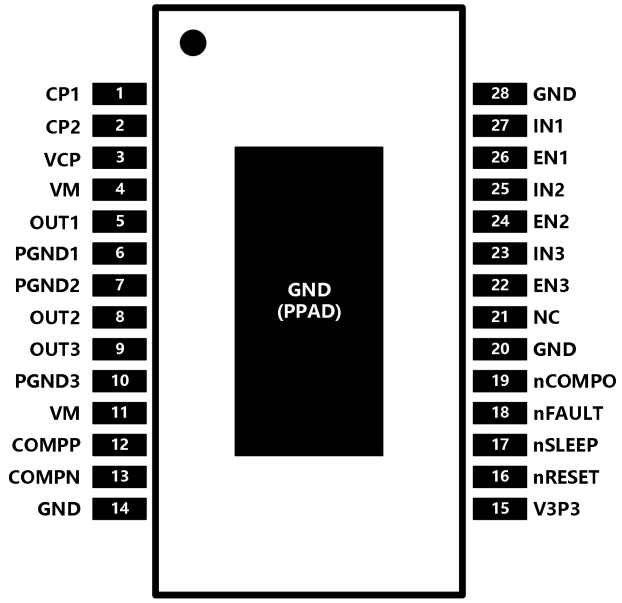

8~35V
MCU或
控制逻辑电路
IN
EN
nSLEEP
nFAULT
3.3V
10mA
AT8313
三路半H桥电机驱动
3.3V LDO
2.5A
BLDC

Version update log

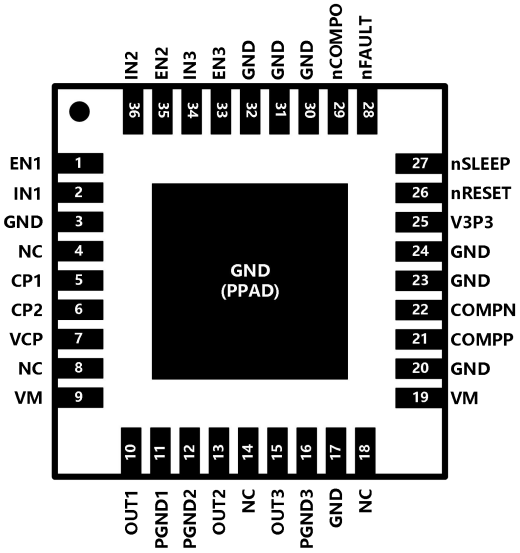
Date	Edition	Content
2020.03	V1.0	Initial version
2020.05	V1.1	1. Update the upper limit of working voltage; 2. Update the upper limit of working temperature; 3. Update the package size.
2021.10	V1.2	Update the QFN package model and tape quantity and packaging specifications

Pin definition

TOP VIEW



TSSOP28



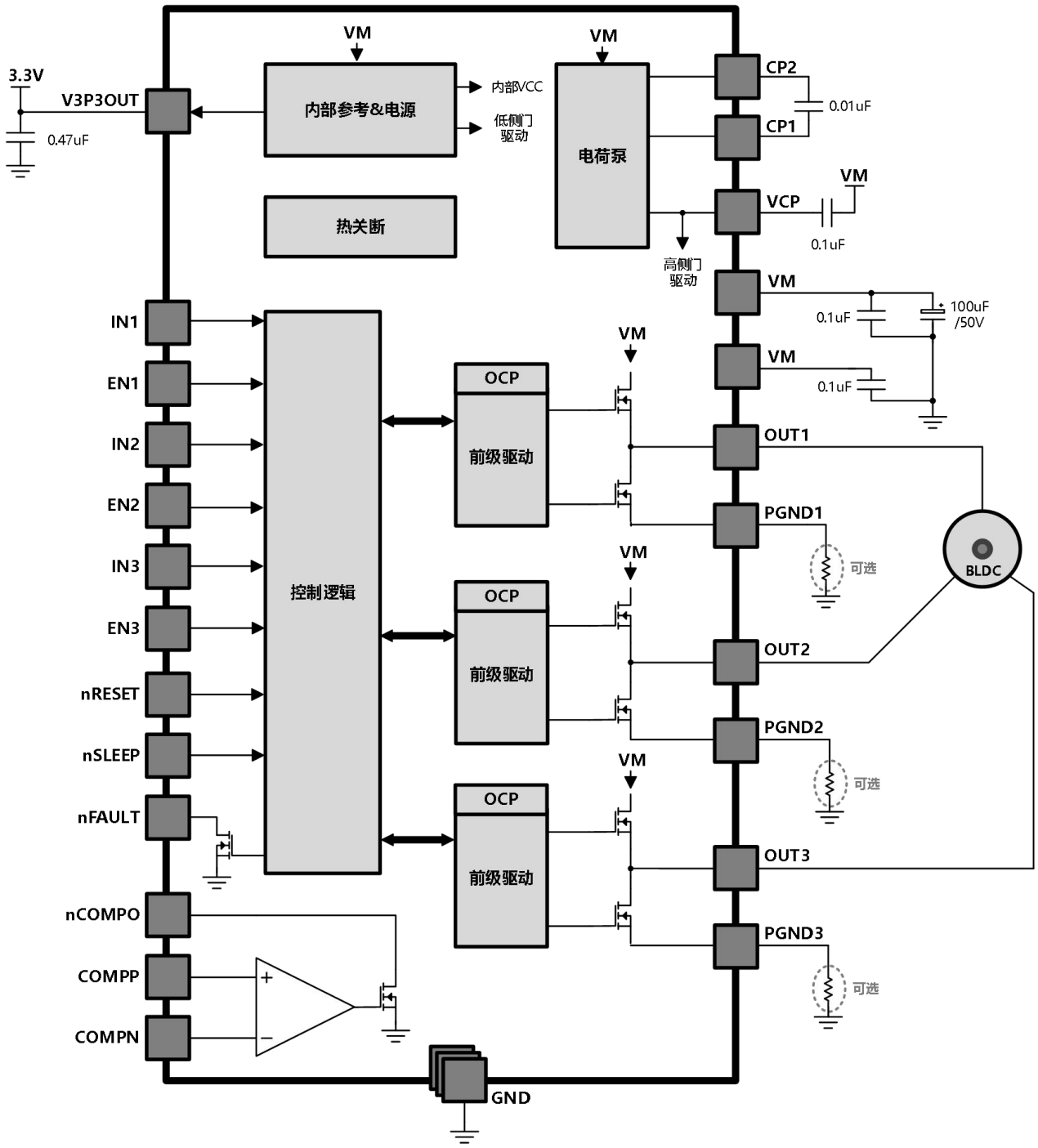
QFN36

Pin list

Pin name	Pin number		Pin description	External components and connections
	ETSSOP	QFN		
Power supply and ground				
GND	14、20、28	3、17、20、23、24、30、31、32	Chip it	All GND pins and bare chip pads should be connected to the system ground
VM	4、11	9、19	Power supply	All VM pins should be connected together and power filtering should be done
V3P3	15	25	3.3V rectifier output	Connect 0.47uF capacitor to ground for filtering
CP1	1	5	Charge pump	Add a 0.01uF capacitor between the two tubes
CP2	2	6		
VCP	3	7	Charge pump	Connect a 0.1uF capacitor to VM
Control input				
EN1	26	1	Enable control input	Logic high level, half H bridge enable output; logic low level, half H bridge output off; built-in pull-down resistor
EN2	24	35		
EN3	22	33		
IN1	27	2	Channel control input	Logic high level, half H bridge output high; logic low level, half H bridge output low; built-in pull-down resistor
IN2	25	36		
IN3	23	34		

nSLEEP	17	27	Sleep mode input	Logic high level, the chip works normally; logic low level, the chip enters sleep mode. Built-in pull-down resistor
nRESET	16	26	Reset input	Logic high level, the chip works normally; logic low level, the chip enters the reset state. Built-in pull-down resistor
Status indication				
nFAULT	18	28	Fault detection indicates output	Open leakage output, if used, need to be connected with an external pull-up resistor. When overtemperature, overcurrent or undervoltage occurs, the output is low level
Output				
PGND1	6	11	Half H bridge low side FET source end	Directly ground or connect the detection current resistance to the ground
PGND2	7	12		
PGND3	10	16		
OUT1	5	10	Half H bridge output	Load the load
OUT2	8	13		
OUT3	9	15		
Comparer				
COMPP	12	21	Comparator positive input	Internal comparator input
COMPN	13	22	Comparator negative input	
nCOMPO	19	29	Comparator output	The internal comparator output is open drain output, and the external needs to be connected with a pull-up resistor
NC	21	4、8、14、18		Suspended or grounded

Functional module block diagram



The working limit of the circuit is at TA = 25 ° C

Parameter	Symbol	Test condition	Scope	Unit
Power supply	VM		-0.3 – 38	V
Output	I_{OUT}		±2.5	A
Output peak current	I_{PEAK}	Internal restrictions	>3	A
Logic input voltage	V_{IN}		-0.3 to 7	V
Half bridge ground voltage	PGNDx		± 0.6	V
Working temperature	T_A	AT8313QNR、AT8313 TPN	-40 to 85	°C
		AT8313QNR-H	-40 to 125	°C
Maximum junction temperature	T_J(max)		150	°C
Storage temperature	T_{stg}		-55 to 150	°C

Thermal resistance characteristic at TA = 25 ° C

Heat metering	QFN 36PINS	ETSSOP 28PINS	Unit
θJA-Thermal resistance coefficient (*) from silicon core to environment	31	33	°C/W

(*) The thermal resistance coefficient of silicon core to the environment under natural convection is obtained by actual test on a JEDEC standard high K circuit board specified in JESD51-7, and environmental conditions are as described in JESD 51-2a.

Recommended working conditions at TA = 25 ° C

Parameter	Symbol	Minimum	Typical case	Maximum	Unit
Power supply (1)	VM	8	-	35	V
Logic input voltage	V_{IN}	0	-	5.25	V
Continuous output current (2)	I_{OUT}	0	-	2.0	A
ENx, INx PWM signal	f_{PWM}	0	-	250	kHz
PGNDx Pin voltage	V_{PGND}	-500	-	500	mV
V3P3, load current	I_{V3P3}	0	-	10	mA

(1) All VM pins must be connected to the same power supply.

(2) When the chip works with large current, do a good job of chip heat dissipation.

Electrical characteristics atTA = 25 ° C, VM= 24 V

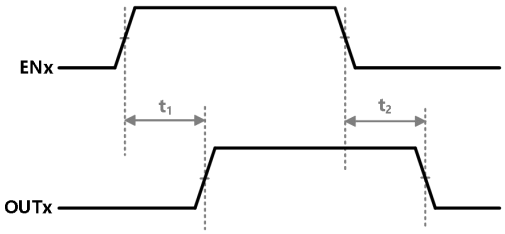
Parameter		Test condition	Minimum	Typical case	Maximum	Unit
Power supply						
I_{VM}	VM Static operating current	f_{PWM} < 50 kHz	-	3	5	mA
I_{VMQ}	VM sleep current	nSLEEP = 0 V	-	350	800	uA
V_{UVLO}	VM under-voltage lock value	VM rise	-	6.5	8	V
Internal rectifier (V3P3)						
V3P3	3.3V rectifier	I_{OUT} = 0 to 10 mA	3.1	3.3	3.5	V
Logical input						
V_{IL}	Low voltage for logical input		-	0.6	0.7	V
V_{IH}	High voltage for logical input		2.2	-	5.25	V
V_{HYS}	Logical input hysteresis		50	-	600	mV
I_{IL}	Logic input current – low level	VIN = 0 V	-2	-	2	uA
I_{IH}	Logic input current – high level	VIN = 3.3 V	-	33	100	uA
R_{PD}	Enter the internal pull-down resistance		-	100	-	kΩ
nFAULT, COMPO output (open drain output)						
V_{OL}	Output low level	I_O = 5 mA	-	-	0.5	V
I_{OH}	Output high level leakage current	V_O = 3.3 V	-	-	1	uA
Comparators (COMPP, COMPN, COMPO)						
V_{CM}	Enter the common-mode voltage range		0	-	4	V
V_{IO}	Input offset voltage		-10	-	10	mV
IIB	Input bias current		-1	-	1	uA
t_R	Response time	100mV step with 10mV overdrive	-	-	2	us
H bridge FETS						
$R_{DS(ON)}$	High side FET on-resistance	I_O = 1A， T_J = 25°C	-	230	-	mΩ
	Low side FET on-resistance	I_O = 1A， T_J = 25°C	-	220	-	
I_{OFF}	Output turn-off leakage current		-2	-	2	uA
Guard circuit						

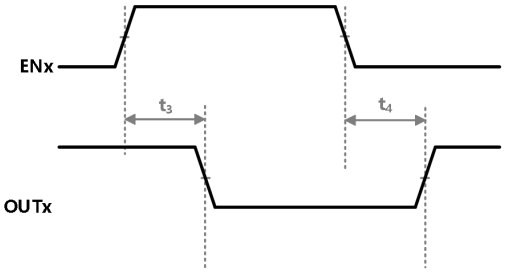
I_{OCP}	Overcurrent peak		3	-	-	A
t_{DEG}	OCP anti-shake delay		-	5	-	us
t_{TSD}	Over temperature threshold	Junction temperature	150	170	180	℃
t_{HYS}	Overtemperature lag		-	45	-	℃
Sleep mode						
t_{WAKE}	Sleep wake time	nSLEEP Rise to half H bridge open	-	500	1000	us

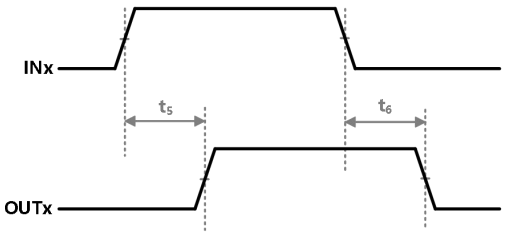
Dynamic timing

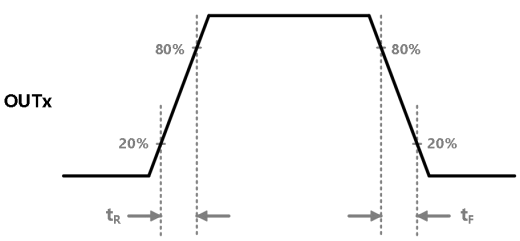
T_A = 25°C, VM = 24 V, R_L = 20 Ω

Parameter	Test condition	Minimum	Typical case	Maximum	Unit
t1 Delay, ENx rises to OUTx rises	INx = 1	100	-	300	ns
t2 Delay, ENx decreases to OUTx decreases	INx = 1	175	-	375	ns
T3 delay, ENx increases and OUTx decreases	INx = 0	50	-	200	ns
T4 delay, ENx decreases and OUTx increases	INx = 0	100	-	300	ns
T5 delay, INx rises to OUTx rises	ENx = 1	300	-	500	ns
T6 delay, INx decreases to OUTx decreases	ENx = 1	275	-	475	ns
The output rise time of the tr is connected to the GND with a resistive load		30	-	150	ns
The output of the tf drops to ground when connected to a resistive load		30	-	150	ns
t_{DEAD} Output dead time		-	150	-	ns



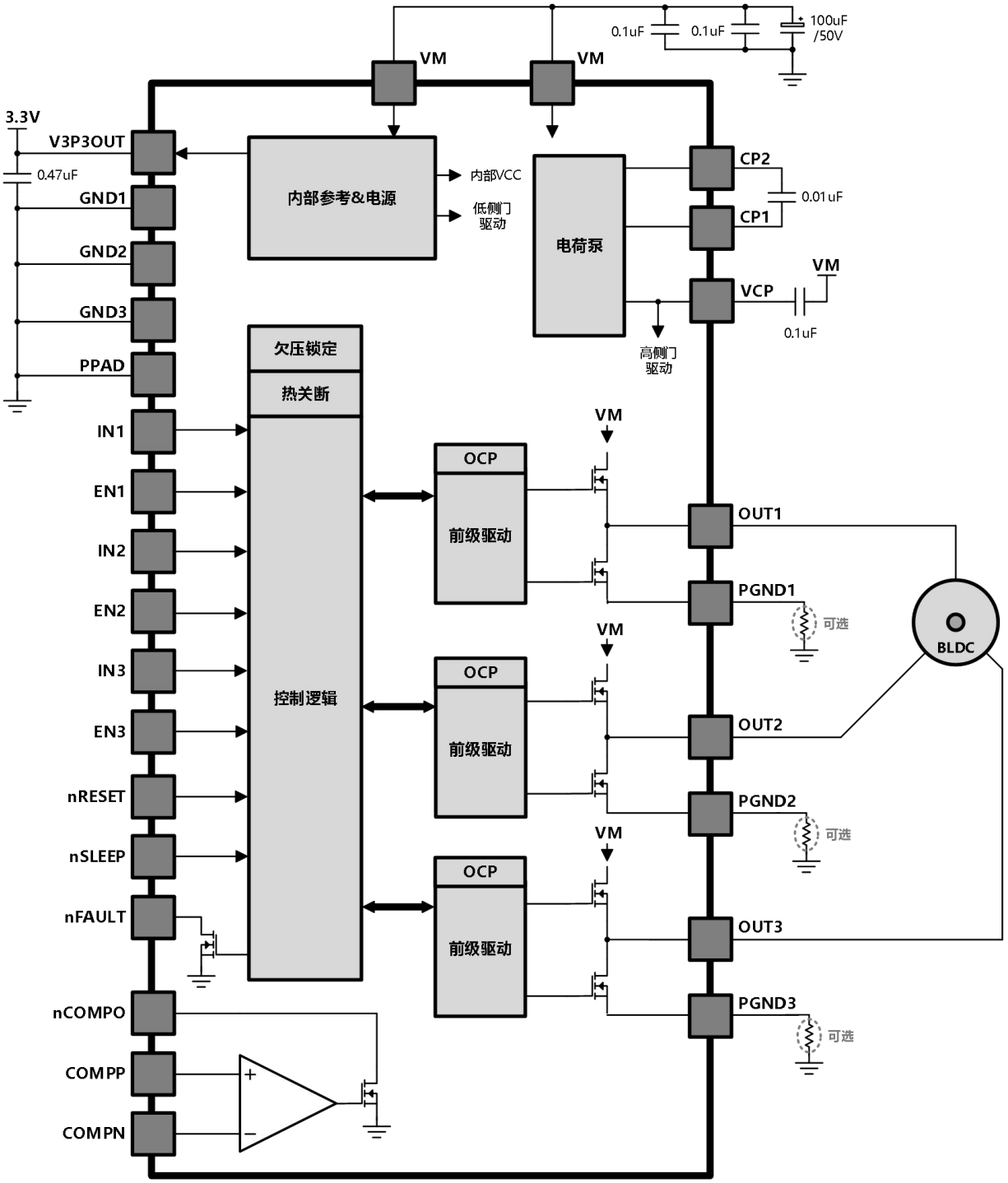






Module function description

AT8313 Integrates three independent half H-bridge to provide 2.5A peak output and 8V-35V single power supply.



output stage

AT8313 includes three half H-bridge drivers. The S terminals of the lower legs MOSFET of each half H-bridge are independent pins (PGND1, PGND2, PGND3), allowing for the connection of three independent shunt resistors. Users can also connect these three pins together and use one shunt resistor to ground; if no shunt is needed, these three pins can be directly grounded.

If a galvanometer resistance is used, ensure that the voltage of these three pins (PGND1, PGND2, PGND3) does not exceed ±500mV.

AT8313 There are two VM pins. Please connect these two pins together to the motor power supply.

H bridge control logic

The input pin INx directly controls the output state OUTx of the half H bridge, and ENx controls the enable of the half H bridge.

ENx	INx	OUTx
0	x	Z
1	1	H
1	0	L

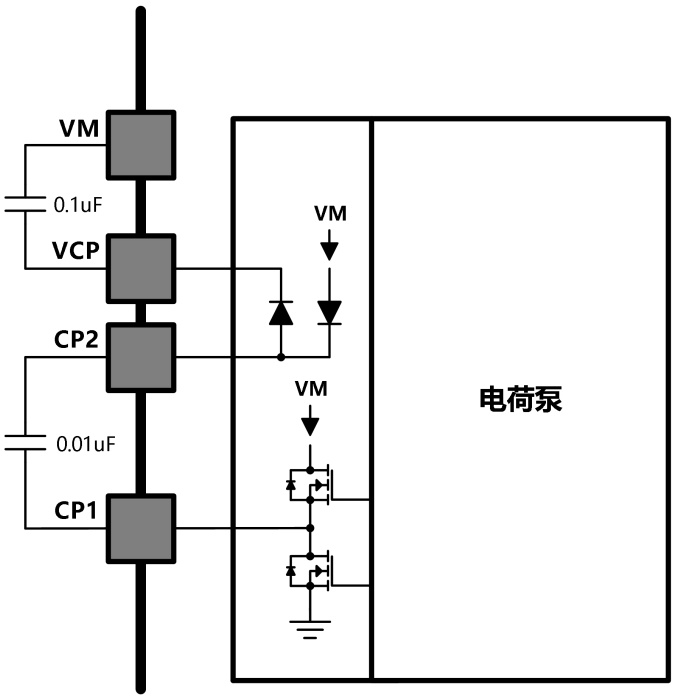
Half H bridge control logic table

charge pump

Since the output stage uses NMOS, a higher gate voltage than the motor supply voltage VM is required to drive this device. AT8313 An internal charge pump circuit generates this voltage.

The charge pump circuit requires two external capacitors to function. See the schematic below.

The charge pump circuit does not work when the nSLEEP pin is input with a low level.

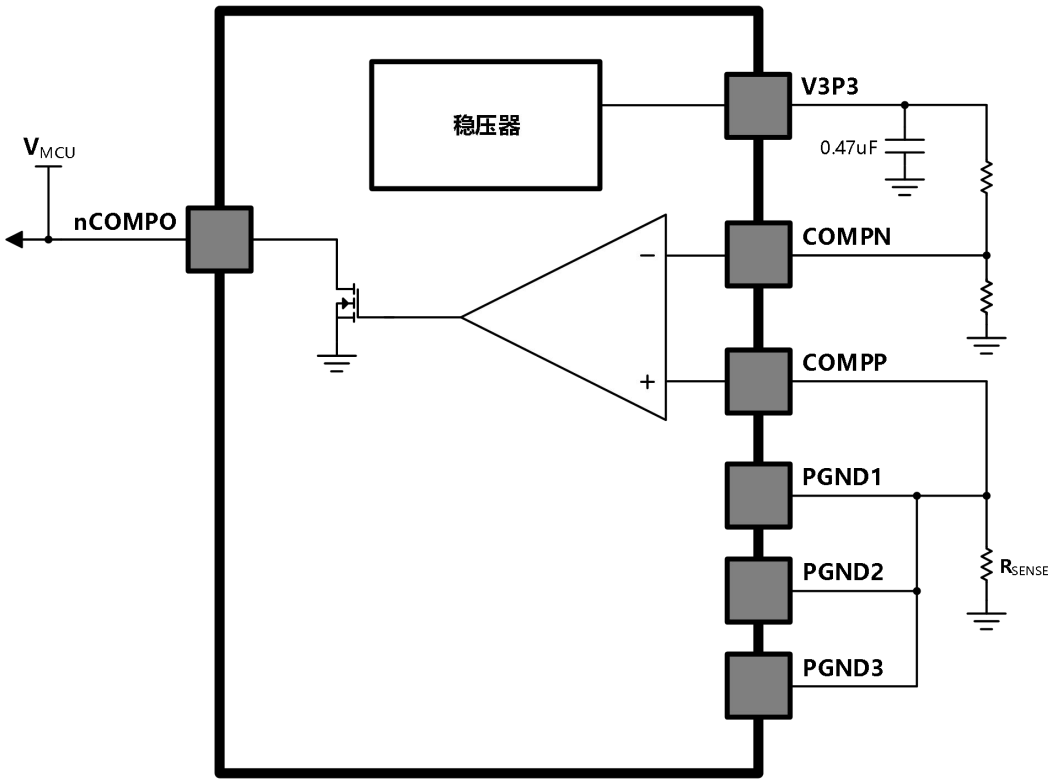


AT8313 Charge pump circuit

comparer

AT8313 A general comparator is built in to limit the output current.

The figure below illustrates the function of using this comparator for current detection to limit current. A sense resistor is used to detect the current flowing through the three half H-bridges' lower tubes. The voltage across this resistor is compared with a set reference level. When the sense voltage exceeds the set value, a current-limiting indicator signal is output to the main controller. An internal 3.3V reference voltage can be used to generate the reference level for this comparator.



The comparator is used for current detection

nSLEEP, nRESET input logic

nRESET When the pin is input low, the chip resets the internal logic and simultaneously disables the half H bridge output. All logical inputs are ignored.

When the nSLEEP pin input is at a low level, the device enters sleep mode, significantly reducing power consumption. After entering sleep mode, the H-bridge of the device is disabled, the charge pump circuit stops working, and all internal clocks cease operation, with all logic inputs being ignored. When the input flips to a high level, the system returns to normal operation. To ensure stable voltage establishment in the internal charge pump, after the nSLEEP returns to a high level and delays for 1ms, normal operations resume. Note: In sleep mode, the 3.3V rectifier circuit continues to operate.

guard circuit

AT8313 Overcurrent protection, overtemperature protection and undervoltage protection.

Overcurrent protection (OCP)

On each MOSFET, there is a current-limiting circuit that detects the current flowing through the MOSFET. If this current reaches the overcurrent threshold and remains for more than the OCP protection time, all MOSFET outputs within the half H-bridge turn off, and the nFAULT pin outputs a low level. To restore normal operation, you need to RESET or SLEEP or power on again.

The flow conditions of the upper and lower pipes on the half H bridge are independently detected. A ground short circuit, a VM short circuit, and a short circuit between the outputs will trigger an overcurrent shutdown.

Overtemperature protection (TSD)

If the junction temperature exceeds the safety threshold, the MOSFET of the half H bridge is prohibited from conducting, and the nFAULT, pin output is low. Once the junction temperature drops to a safe level, the chip will automatically return to normal.

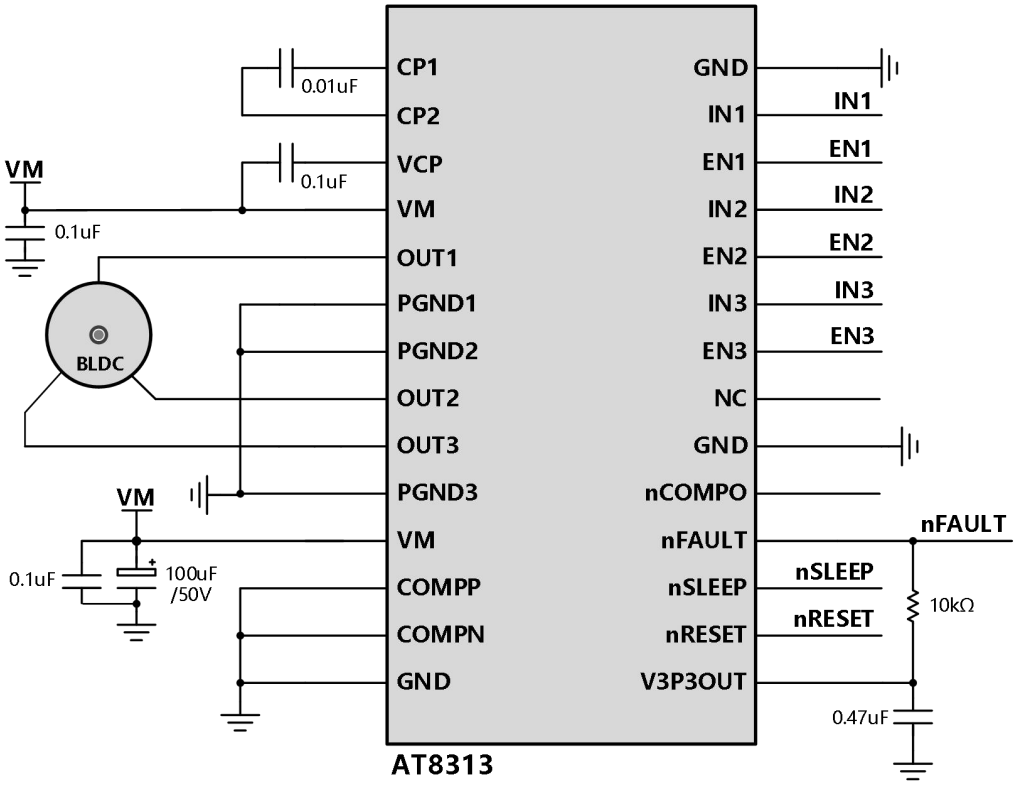
Under-voltage lockout protection (UVLO)

At any time, if the voltage on the VM pin drops below the under-voltage lockout threshold, all internal circuits will be disabled and reset. When the voltage on the VM rises above UVLO, all functions automatically resume. In the event of an under-voltage condition, the nFAULT pin

outputs a low level.

Information on circuit applications

AT8313 Can drive a brushless DC motor, brushed DC motor or other inductive loads. Brushless DC motor control



A brushless DC motor generally operates at a specific voltage, such as 12V or 24V. To achieve the same power output, the higher the operating voltage, the lower the required current. A higher operating voltage also facilitates achieving a higher speed. AT8313 recommends a maximum operating voltage of 35V.

Generally speaking, working at a relatively low voltage makes it easier to obtain more accurate current control. AT8313 Minimum support for 8V operation.

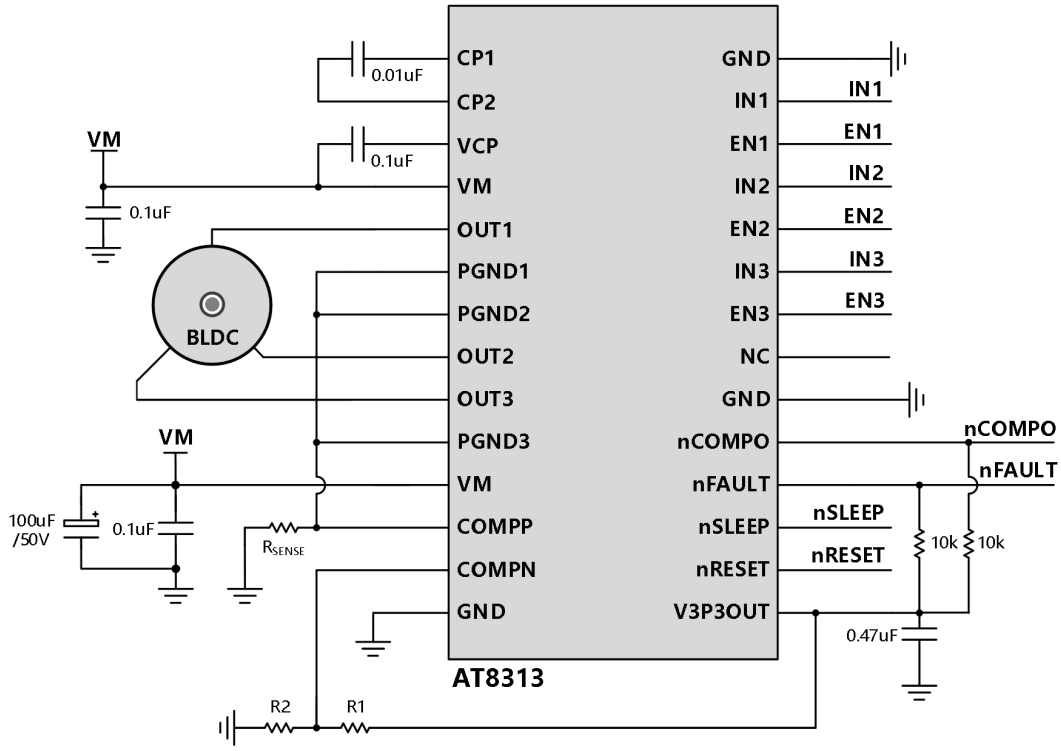
By controlling three independent half H-bridges, the AT8313 can achieve trapezoidal (120°) or sinusoidal (180°) output. At the same time, the AT8313 can perform both synchronous and asynchronous rectification. Synchronous rectification is achieved by adding PWM to INx, while asynchronous rectification is realized by adding PWM to ENx.

State	OUT1 (PHASE U)			OUT2 (PHASE V)			OUT3 (PHASE W)		
	IN1	EN1	OUT1	IN2	EN2	OUT2	IN3	EN3	OUT3
1	X	0	Z	1	1	H	0	1	L
2	1	1	H	X	0	Z	0	1	L
3	1	1	H	0	1	L	X	0	Z
4	X	0	Z	0	1	L	1	1	H
5	0	1	L	X	0	Z	1	1	H
6	0	1	L	1	1	H	X	0	Z
Stop a vehicle	0	1	L	0	1	L	0	1	L

by appl-ying the brake									
Glissade	X	0	Z	X	0	Z	X	0	Z

Trapezoidal control

DC brushless control with current detection



In this example, when the potential of COMPP and COMPN is the same, a jump occurs in the COMPO level.

The peak current is calculated by the following formula:

$$I_{TRIP} = \frac{COMPN}{R_{SENSE}}$$

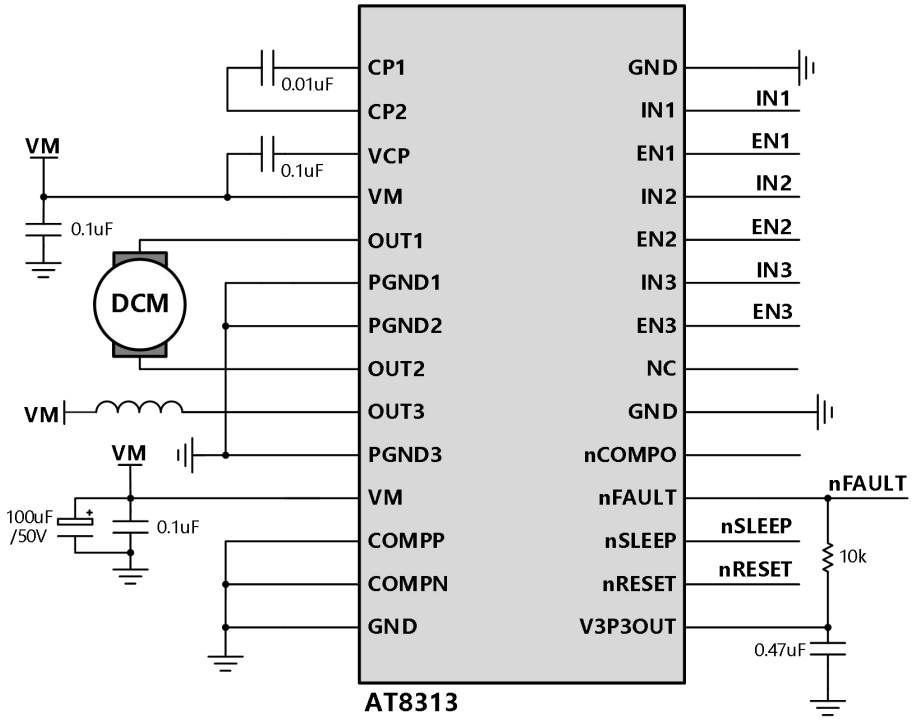
Assuming the target peak current is 2.5A and RSENSE is 200mΩ, the voltage of COMPN should be set to 0.5V.0.5V is divided from V3P3 (3.3V), so R1 is 56kΩ and R2 is 10kΩ.

SENSE Selection of resistance:

Surface mount packaging, low sensitivity, sufficient power, close to the chip pins.

Because the power resistor is large in size and expensive, another approach is to use three small volume resistors in parallel.

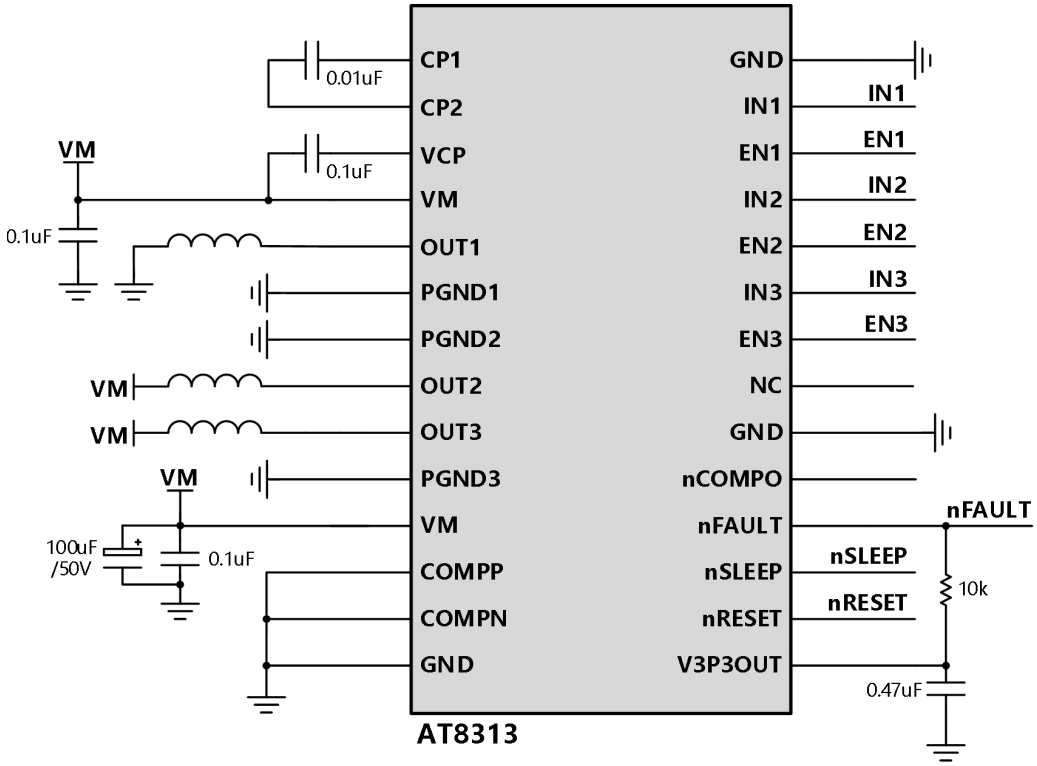
Brushed motor and solenoid load control



EN1	IN1	EN2	IN2	OUT1	OUT2	Function
1	1	1	0	H	L	Forward direction
1	0	1	1	L	H	Opposite direction
1	0	1	0	L	L	Brake (slow decay on the lower side)
1	1	1	1	H	H	High side slow atte-nuation
0	X	0	X	Z	Z	Glissade

True value table of brushed motor control

Three solenoid loads



IN2	EN2	OUT2	Function
X	0	Z	Shut down (roll)
1	1	H	Stop a vehicle by applying the brake
0	1	L	Open

High side load control

IN1	EN1	OUT1	Function
X	0	Z	Shut down (roll)
1	1	H	Open
0	1	L	Stop a vehicle by applying the brake

Low side load control

Map layout notes

A large heat sink should be placed on the PCB board, and a wide ground wire should be connected to the ground. In order to optimize the electrical characteristics and thermal performance of the circuit, the chip should be directly attached to the heat sink.

For the electrode power supply VM, an electrolytic capacitor of no less than 47uF should be coupled to the ground. The capacitor should be placed as close to the device as possible.

In order to avoid the capacitance coupling problem caused by high speed dv/dt transformation, the wiring at the output end of the drive circuit should be far away from the wiring at the logic control input end. The lead wire at the logic control end should use low impedance routing to reduce the noise caused by thermal resistance.

Ground wire setting

All ground lines in the chip should be connected together, and the connections should be as short as possible. A star-diffused ground line located under the device will be an optimized design.

Adding a copper heat sink under the laid ground will better optimize the circuit performance.

Current sampling Settings

To reduce errors caused by parasitic resistance on the ground wire, the sampling resistor RS for motor current should be grounded separately to minimize errors from other factors. The separate ground wire must ultimately connect to a star-distributed ground bus, with this connection as short as possible. For small-value Rs, the voltage drop V = I × RS is 0.5V, making the voltage drop across the PCB connection negligible at 0.2V; this point must be taken into account.

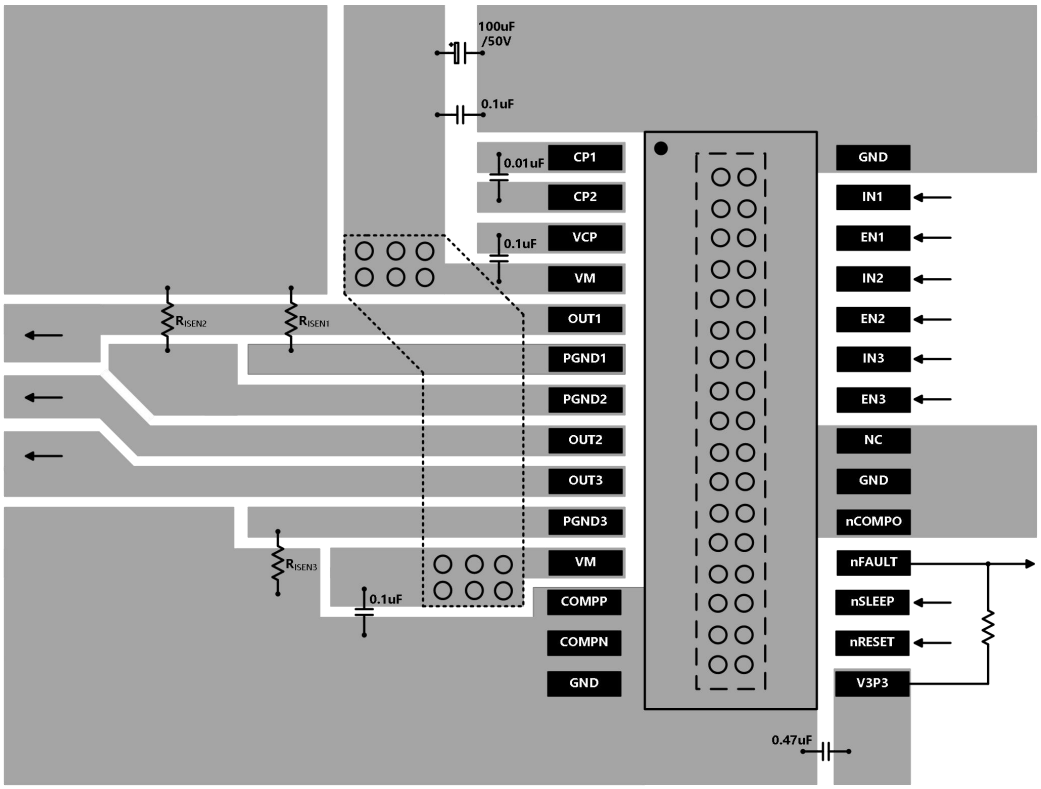
PCB should avoid using test transfer sockets as much as possible. The connection resistance of the test socket may change the size of Rs, causing errors in the circuit. The value of Rs is selected according to the following formula:

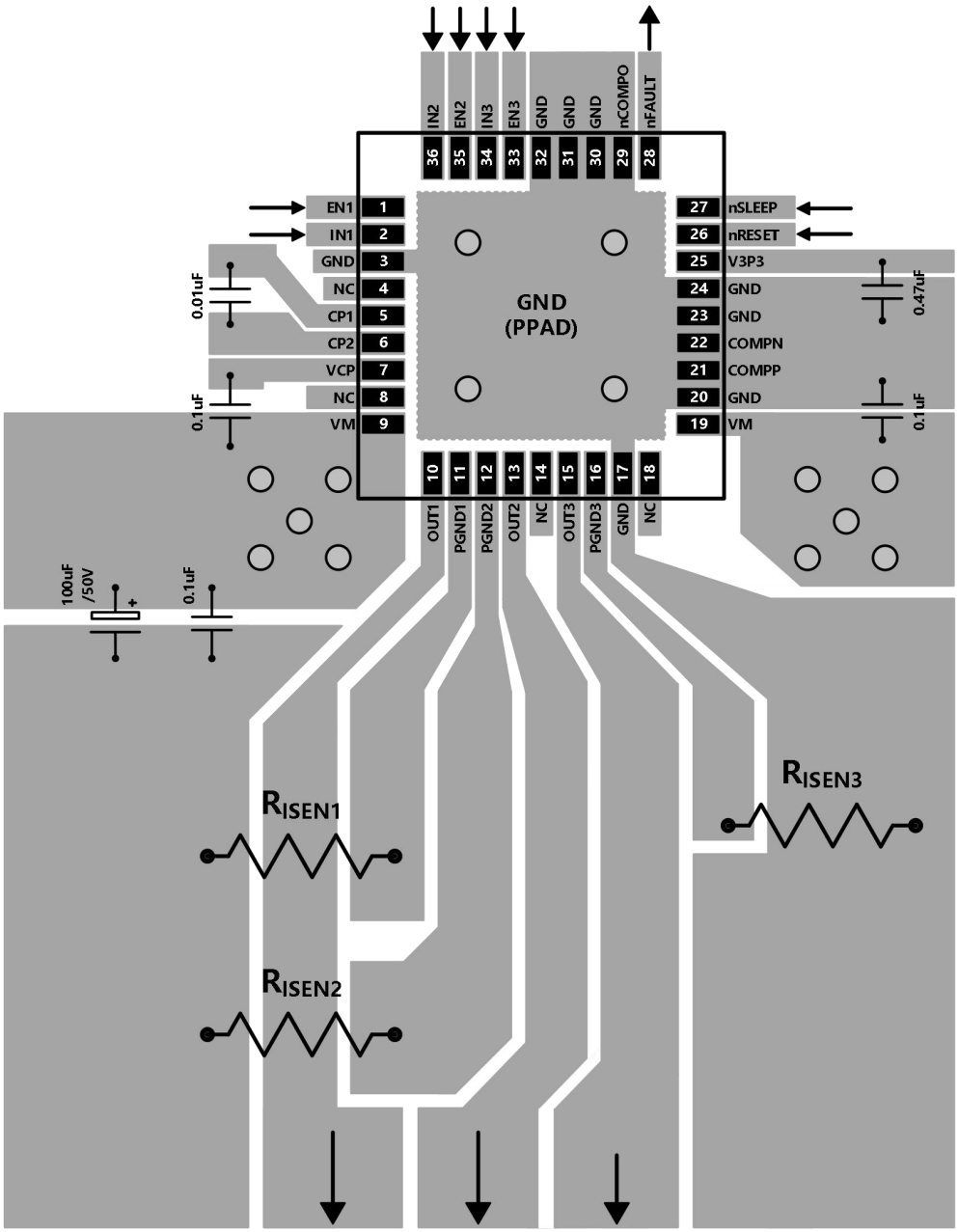
$$R_S = 0.5 / I_{TRIP\max}$$

Thermal protection

When the junction temperature of the internal circuit exceeds 170 , the overtemperature module starts to work and all the internal drive circuits are shut down. The overtemperature protection circuit only protects the problems caused by the excessive temperature of the circuit, but should not affect the output short circuit. The threshold window size of thermal shutdown is 45 .

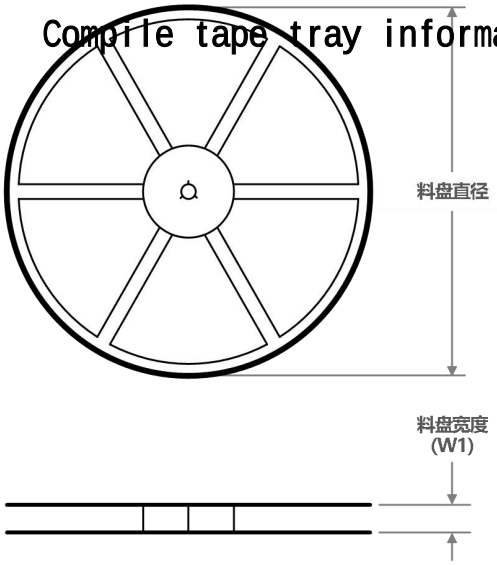
PCB layout example

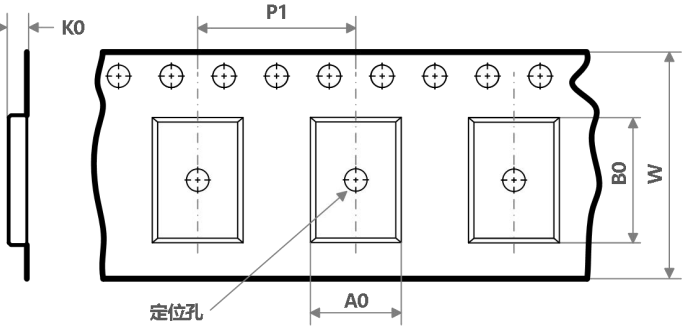

100uF
/50V
0.1uF
0.01uF
CP1
CP2
0.1uF
VCP
VM
OUT1
PGND1
PGND2
OUT2
OUT3
PGND3
VM
COMPP
COMPN
GND
RISEN2
RISEN1
RISEN3
0.1uF
GND
IN1
EN1
IN2
EN2
IN3
EN3
NC
GND
nCOMPO
nFAULT
nSLEEP
nRESET
V3P3
0.47uF



PCB layout example

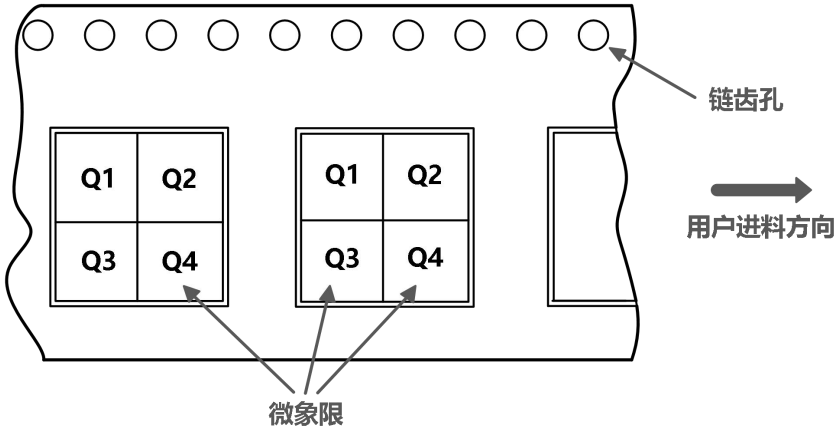
Compile tape tray information





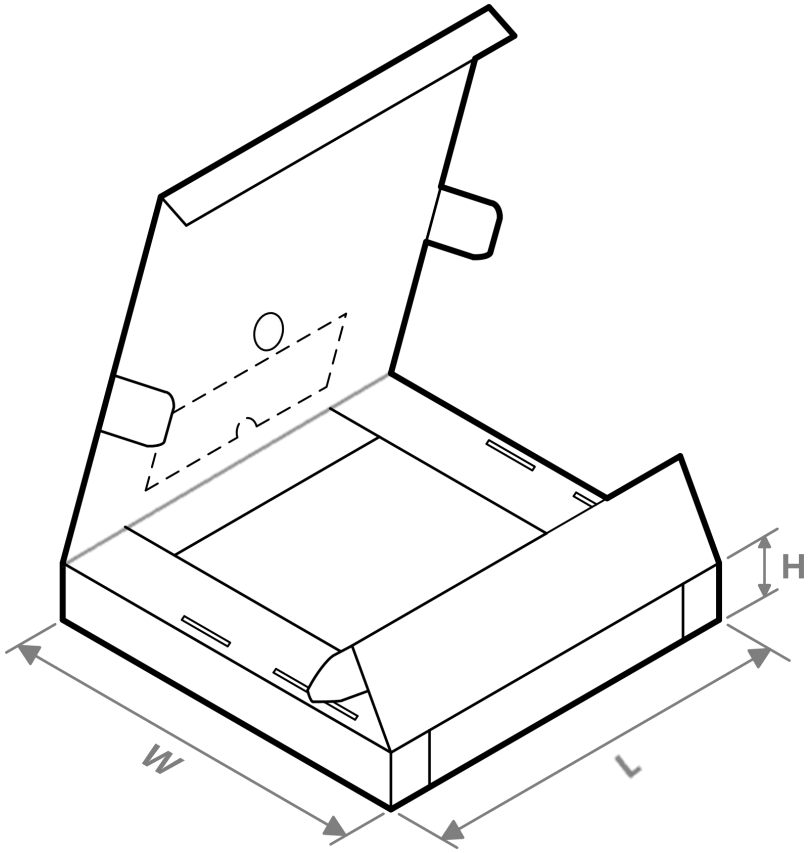
A0	Bin width
B0	Length of trough
K0	Bin thickness
W	Overall width of the carrier
P1	Center spacing of adjacent slots

Bandage PIN 1 Quadrant allocation



Package Type	Package Characteristic	Number of pins	SPQ	Charging tray Diameter (mm)	Charging tray Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
AT8313 QNR	QFN	QNR	36	3000	330	16.4	6.3	6.3	1.1	12	16	Q2
AT8313 QNR-H	QFN	QNR-H	36	3000	330	16.4	6.3	6.3	1.1	12	16	Q2
AT8313 TPN	ETSSOP	TPN	28	3000	330	16.4	6.8	10.1	1.6	8	16	Q1

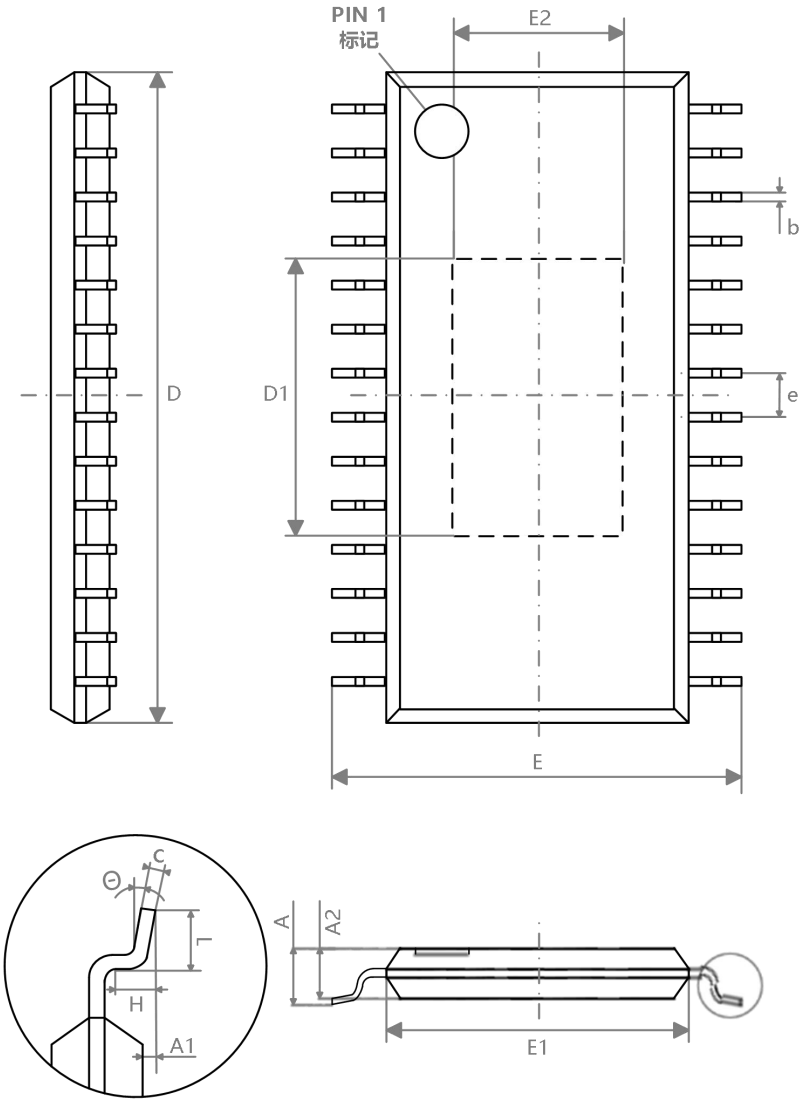
Band material tray packaging size



Device	Packaging type	Packaging identification	Number of pins	SPQ	Length (mm)	Width (mm)	Altitude (mm)
AT8313 QNR	QFN	QNR	36	3000	350	340	50
AT8313 QNR-H	QFN	QNR-H	36	3000	350	340	50
AT8313 TPN	ETSSOP	TPN	28	3000	350	340	50

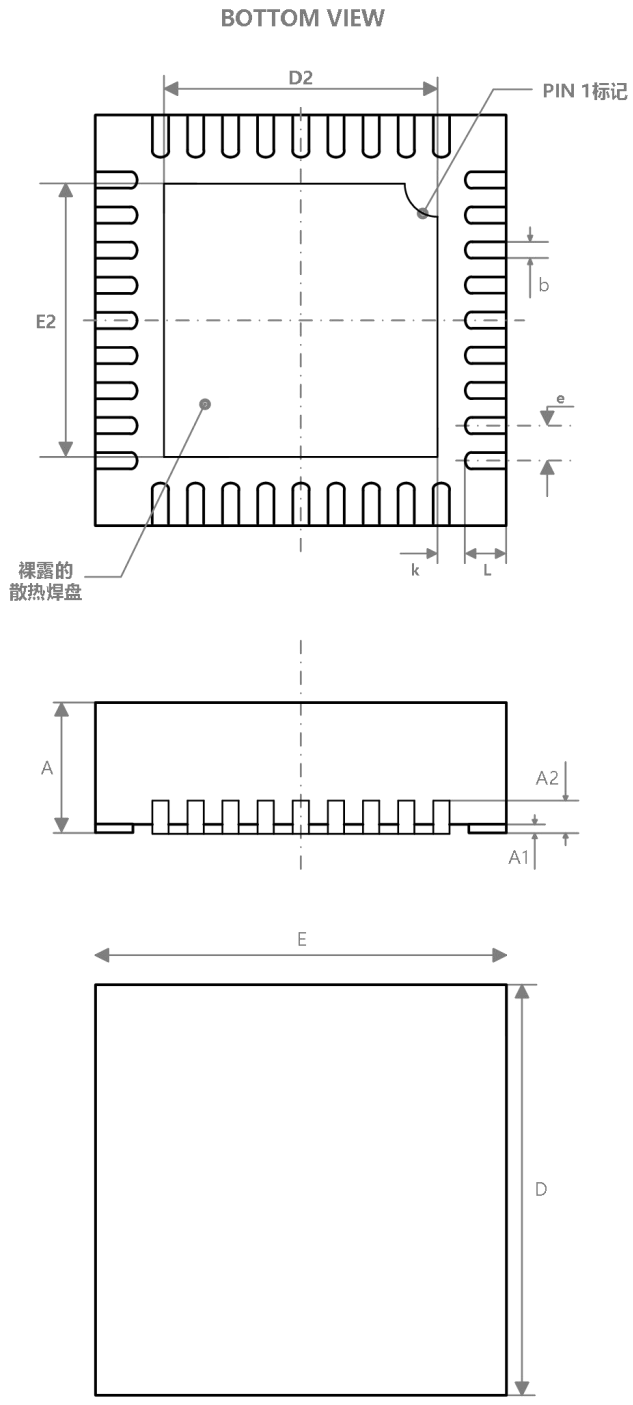
Package information

ETSSOP28



Symbol	Millimetre (mm)	
	Minimum	Maximum
D	9.60	9.80
D1	5.4	5.6
E	6.20	6.60
E1	4.30	4.50
E2	2.60	2.80
A	-	1.20
A1	0.05	0.15
A2	0.80	1.00
b	0.20	0.29
c	0.13	0.18
e	0.65(BSC)	
L	0.45	0.75
H	0.25(TYP)	
θ	0°	8°

QFN36



Symbol	Millimetre (mm)	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A2	0.203(REF)	
D	5.95	6.05
D2	4.05	4.25
E	5.95	6.05
E2	4.05	4.25
b	0.20	0.30
e	0.50(TYP)	
k	0.375(REF)	
L	0.50	0.60