description

AT8837 provides an integrated motor driver solution for low-voltage applications such as cameras, smart locks, and toys, or battery-powered products. AT8837 can drive a brushed DC motor or inductive loads like solenoids, offering up to 1A of drive current. The device operates within a power supply voltage range of 2.7-12V and includes comprehensive protection features such as overcurrent, short circuit, overtemperature, and undervoltage lockout.

AT8837 It has a PWM (IN1/IN2) input interface.

AT8837 Provide a DFN-8 (2mm*2mm) package with exposed pads, and it is lead-free product, which meets the environmental protection requirements.

characteristic

Independent H-bridge drive circuit

Drive a DC brushed motor or other inductive load

Low RDS (ON) resistance, 1.05Ω (HS + LS)

Continuous drive output of 1A

Wide voltage supply range, 2.7-12V

nSLEEP Low power sleep mode controlled by the pin

overcurrent protection

Overtemperature shutdown circuit

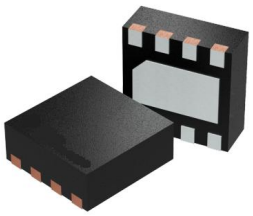
short-circuit protection

Under-voltage lockout protection

Appl y

- Camera consumer products
- toys
- Robotic smart door bells

Packaging form

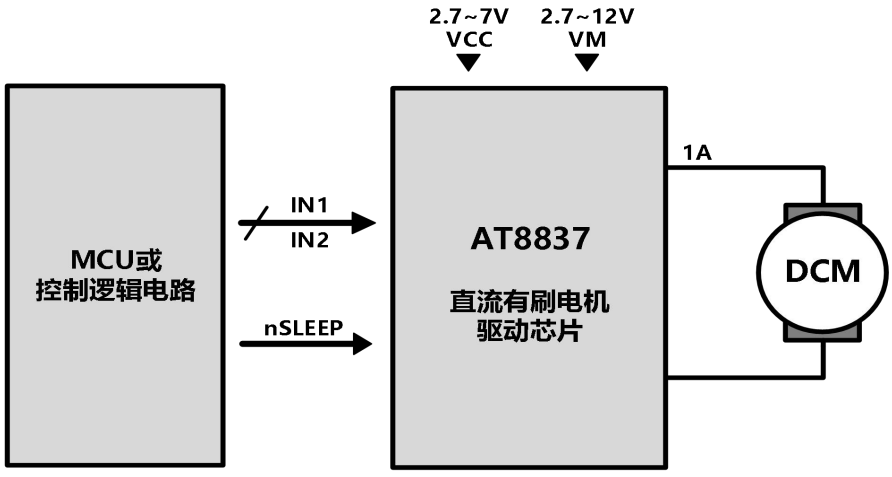


DFN-8 with PAD

Model selection

Order number	Package	Pack
AT8837	DFN2*2-8	Strips, 3000 beads per disc

Typical application schematic



Version update log

Date	Edition	Content
2018.04	V1.0	Initial version
2018.09	V1.1	Power supply voltage lower limit correction
2018.12	V1.2	Correction of voltage rating of power filter capacitor
2020.03	V1.3	1. Modify the upper limit of power supply voltage; 2. Add packaging information; 3. Increase the thermal resistance parameter; 4. Add a table of temperature characteristics for test waveforms and conduction impedance
2020.09	V1.4	Modify the POD size of the package

The working limit of the circuit is at TA = 25 ° C

Parameter	Symbol	Condition	Scope	Unit
Motor power supply voltage	VM		-0.3 – 15	V
Continuous output current	I_{OUT}		±1	A
Instantaneous peak current	I_{PEAK}	Internal restrictions	>1.5	A
Logic power supply voltage	VCC		-0.3 to 7	V
Logic input voltage	V_{IN}		-0.5 to VCC	V
Operating ambient temperature	T_A		-40 to 85	°C
Maximum junction temperature	$T_{J(max)}$		150	°C
Storage temperature	T_{STG}		-55 to 150	°C

Thermal resistance characteristic at Ta = 25 ° C

Heat metering	DFN 8PINS	Unit
θJA-Thermal resistance coefficient (*) from silicon core to environment	50	°C/W

(*) The thermal resistance coefficient of silicon core to the environment under natural convection is obtained by actual test on a JEDEC standard high K circuit board specified in JESD51-7, and environmental conditions are as described in JESD 51-2a.

Recommended working conditions at TA = 25 ° C

Parameter	Symbol	Minimum	Typical case	Maximum	Unit
Motor power supply voltage	VM	2.7	-	12	V
Logic power supply voltage	VCC	2.7	-	5.25	V
Continuous output current	I_{OUT}	0	-	0.8	A
Enter the PWM frequency	f_{PWM}	0	-	250	kHz

(1) All voltage values are based on the ground port as the potential zero point.

(2) When the chip works with large current, do a good job of chip heat dissipation.

(3) The performance of the chip is not guaranteed when it operates under conditions other than those recommended.

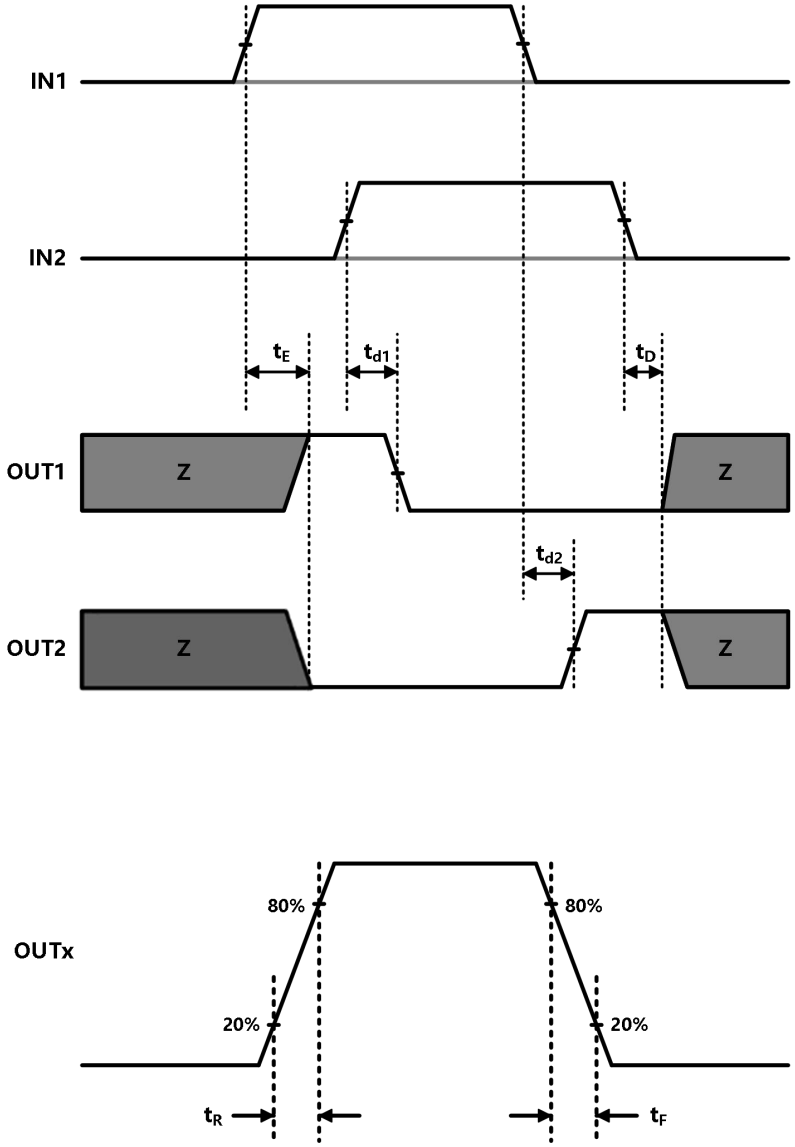
(4) When the chip works beyond the circuit limit, it may cause permanent damage to the device.

(5) If the chip is placed for a long time beyond the operating limit of the circuit, it may affect the reliability of the device.

Electrical characteristics atTA = 25 °C, VM= 5 V, VCC = 3.3 V

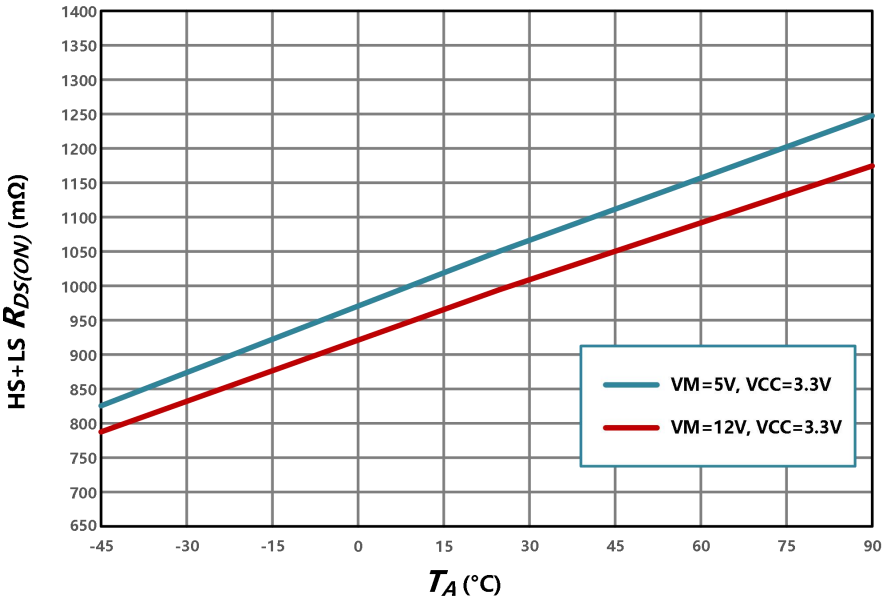
Parameter		Test condition	Minimum	Typical case	Maximum	Unit
Power supply						
I_{VM}	VM Static operating current			0.3	0.8	mA
I_{VMQ}	VM sleep current	nSLEEP = 0		50	100	nA
I_{VCC}	VCC static operating current			0.8	1.5	mA
I_{VCCQ}	VCC sleep working current	nSLEEP = 0		0.3	1	uA
Logical input						
V_{IL}	Low voltage for logical input				0.8	V
V_{IH}	High voltage for logical input		2.0			V
V_{HYS}	Logical input hysteresis			0.24		V
I_{IL}	Logic input current – low level	V_{IN} = 0			1	uA
I_{IH}	Logic input current – high level	IN1, IN2		30		uA
		nSLEEP		30		uA
R_{PD}	Enter internal pull-down resistance	nSLEEP		100		KΩ
		IN1, IN2		100		KΩ
H bridge FETs						
$R_{DS(ON)}$	High side FET on-resistance	I_O = 200mA		700		mΩ
	Low side FET on-resistance	I_O = 200mA		350		
I_{OFF}	Output turn-off leakage current		-1		1	uA
Guard circuit						
I_{OCP}	Overcurrent protection threshold		1.2	1.35		A
t_{DEG}	OCP anti-shake delay			3		us
T_{RETRY}	OCP reboot time			1.3		ms
T_{TSD}	Over temperature threshold	Chip internal junction temperature	150	160	180	℃
V_{UVLO}	VCC under-voltage lock value	VCC rise		2.6		V
$V_{UVLOHYS}$	VCC under-voltage hysteresis			100		mV
Resting state						
t_{WAKE}	Sleep wake time	Pull up nSLEEP to bridge H		35		us

t_E	Output enable time	Output enable time		325	500	ns
t_D	Output turn-off time	Output disable time		200	500	ns
t_{d1}	Input changes to output with low delay	Delay time，IN2 high to OUT1 low		300	500	ns
t_{d2}	The input change takes a long time to go to the output	Delay time，IN1 low to OUT2 high		400	500	ns
t_R	Rise time	22Ω to GND, 20% to 80%		20	180	ns
t_F	Drop-out time	22Ω to GND, 80% to 20%		5	180	ns
t_{DEAD}	Dead zone time			205		ns

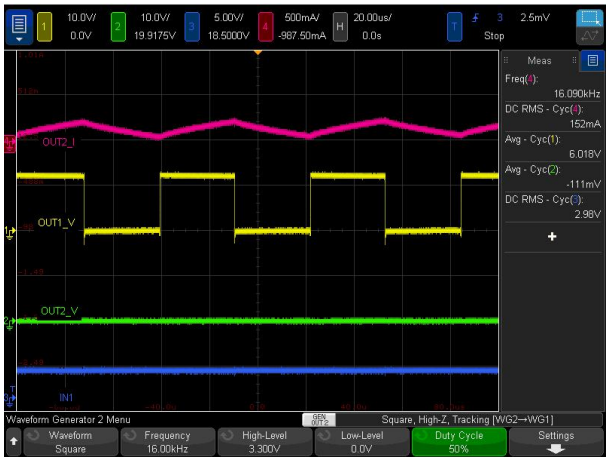


Time parameter diagram

Typical work characteristic curve

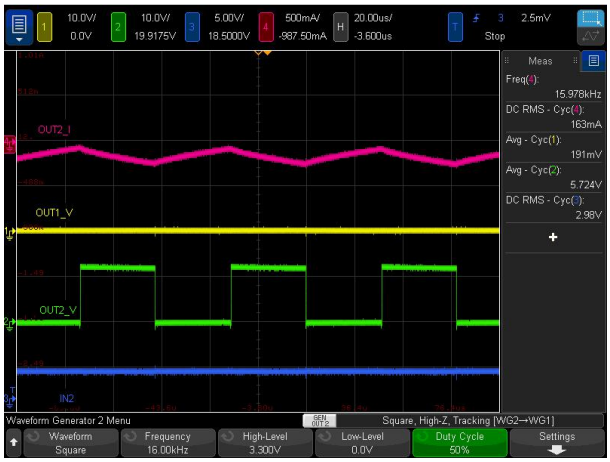


* The chart is generated using feature data

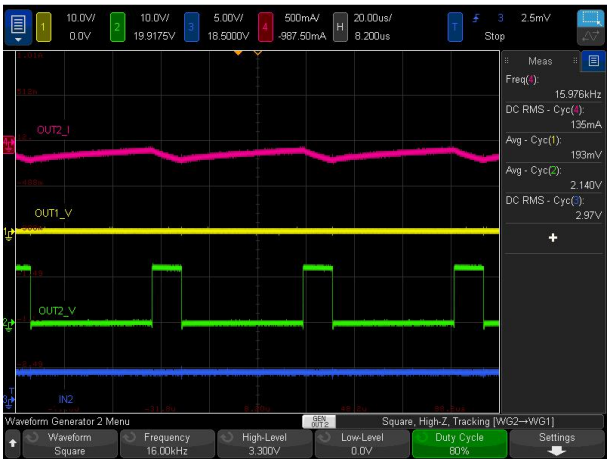


50% duty cycle, positive

20% duty cycle, positive



50% duty cycle, reverse

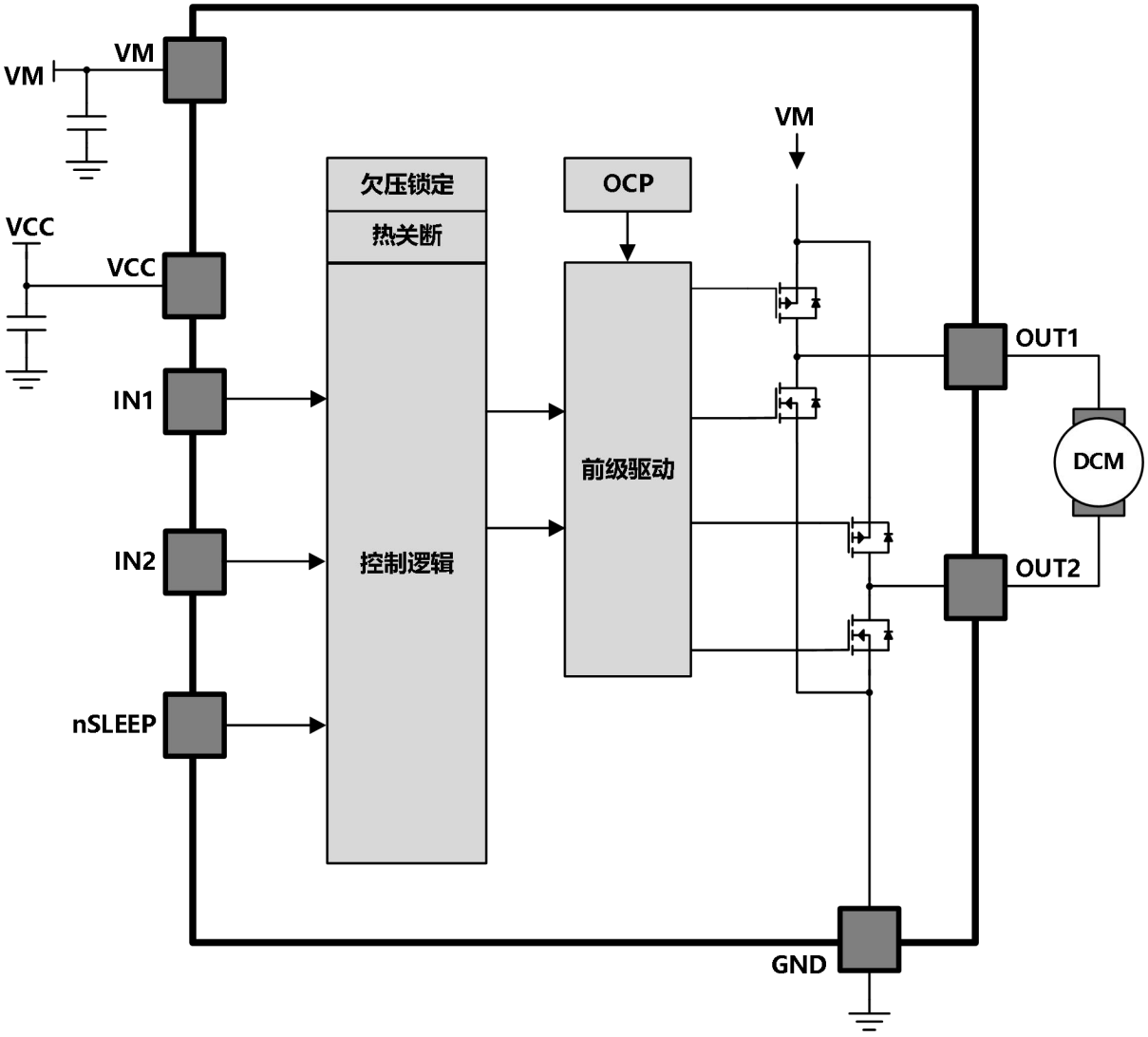


20% duty cycle, reverse

Module function description

AT8837 provides an integrated drive solution for single brushed DC motors or inductive loads such as solenoids. The chip internally integrates a H-bridge power output module, delivering a peak current output of 1A. AT8837 operates within a normal voltage range of 2.7 to 12V. By pulling down the nSLEEP pin, AT8837 can achieve low-power sleep mode.

The chip integrates the power tube and its control circuit, reduces the number of peripheral devices, and has complete protection functions such as overcurrent, short circuit, overheating and undervoltage lock.



functional block diagram

H bridge control logic

The input pins IN1 and IN2 control the enable and current direction of the H bridge. The following table shows the logical relationship between them.

nSLEEP	IN1	IN2	OUT1	OUT2	Function (DC motor)
0	X	X	Z	Z	Dormancy
1	0	0	Z	Z	Glissade
1	0	1	L	H	Reversal
1	1	0	H	L	Corotation
1	1	1	L	L	Stop a vehicle by applying the brake

H Bridge control logic table

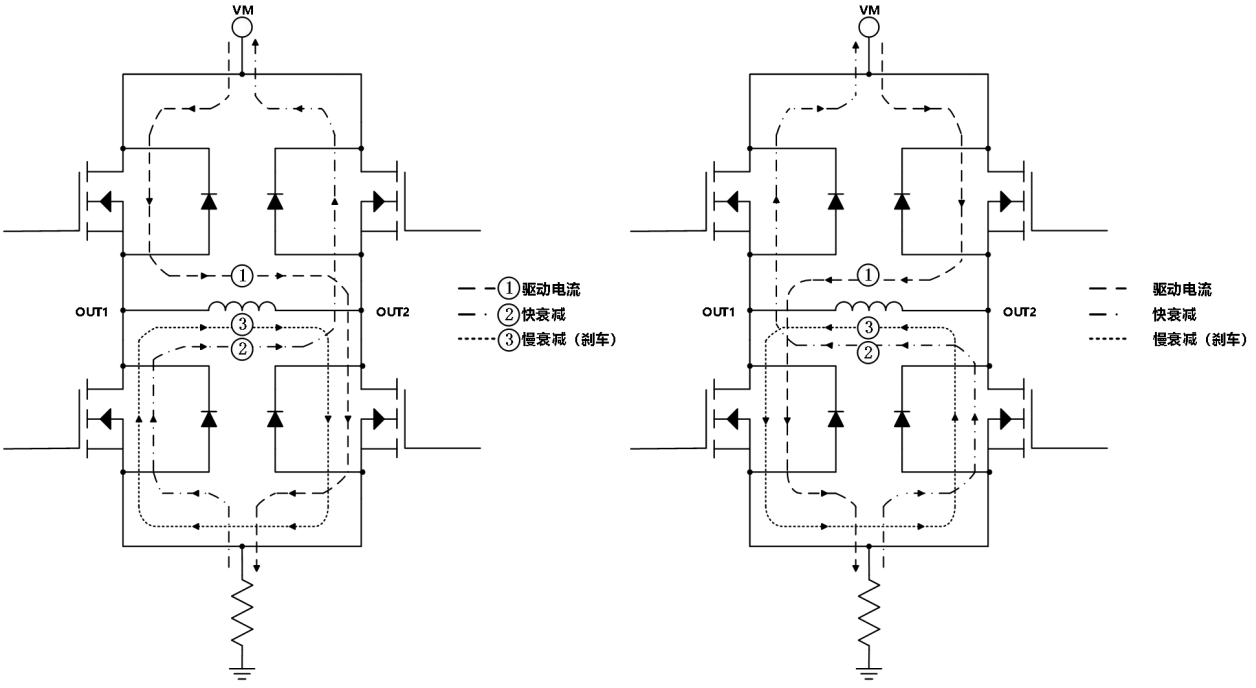
The logic input can also use PWM control to achieve speed regulation. When a PWM wave controls a coil, the drive current is interrupted, and due to the inductive characteristics of the motor, the motor coil must continue to conduct. To operate the motor coil to continue conducting, the H-bridge can operate in two different states: fast decay or slow decay. In fast decay mode, the H-bridge turns off, and the freewheeling current flows through the body diode; in slow decay mode, the ends of the motor coil are short-circuited.

When PWM control is used in fast attenuation mode, the PWM signal controls one INx pin while the other pin remains low; when used in slow attenuation mode, one of the pins remains high.

IN1	IN2	Function
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

PWM controls motor speed

The following figure shows the current path in different drive and attenuation modes.



Drive and decay mode

Overcurrent protection (OCP)

On each FET, there is a current detection circuit. When the current exceeds the set threshold and persists for more than the OCP anti-flicker time tDEG, all FETs in the H-bridge turn off. After a period of overcurrent reset tRETRY, the H-bridge will open again. If the overcurrent is cleared, the H-bridge resumes normal operation; if the overcurrent persists, the aforementioned action repeats.

Overcurrent protection is triggered if the upper and lower pipes of H bridge are short-circuited to ground, to VM, or to the output.

Overtemperature protection (TSD)

If the junction temperature exceeds the safety threshold, all FETs in the H bridge will be turned off. After the junction temperature drops to a certain value, the chip will automatically return to normal operation.

Under-voltage lockout protection (UVLO)

If the voltage on the VCC pin is below the undervoltage lockout threshold, all FETs in the internal H-bridge are turned off. When the VCC rises above the undervoltage lockout threshold, the chip automatically returns to normal operation.

Device protection threshold

Abnormal conditions	Trigger conditions	H bridge	Recover
VCC Under-voltage Lockout Protection (UVLO)	VCC < 2.55V	Turn-off	VCC > 2.65V
Overcurrent, short circuit protection (OCP)	I_{OUT} > 1.2A(MIN)	Turn-off	After 1.2ms
Thermal shutdown (TSD)	T_J > 160 ℃(MIN)	Turn-off	T_J < 140 ℃

Abnormal condition table

Device function mode

nSLEEP When the nSLEEP pin is input at a low level, the device enters low-power sleep mode. After entering low-power sleep mode, the H-bridge of the device is turned off and all logic inputs are ignored; when the nSLEEP pin is input at a high level, the chip returns to normal operation.

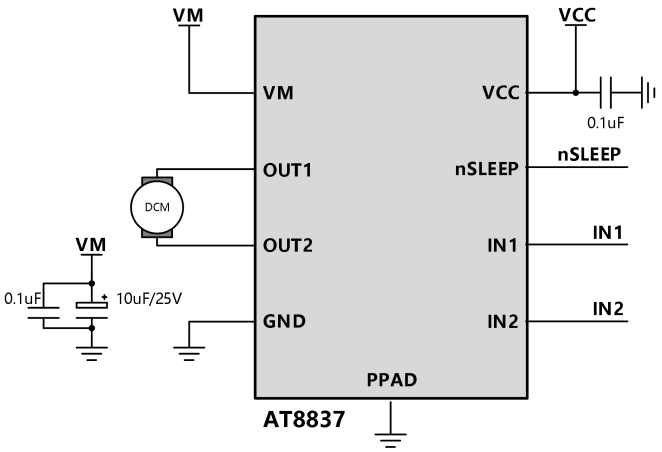
It is recommended to pull all input pin levels to low level when entering low power sleep mode in order to further reduce chip power consumption.

Pattern	Condition	H bridge
Regular work	nSLEEP = 1	Regular work
Sleep mode	nSLEEP = 0	Turn-off
An exception occurred	Meet any exceptional conditions	Turn-off

Function mode table

Information on circuit applications

Brushed DC motor drive



Typical design requirements

Design value	Refer to	Example values
Motor power supply voltage	VM	12V
Logic power supply voltage (only AT 8837)	VCC	5V
Target current RMS	I_{OUT}	0.5A

Typical application

Detailed design process

power dissipation

The power consumption of AT8837 is mainly on the impedance RDS (ON) of the FET in the H bridge.

The average power consumption can be roughly estimated as:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

In the formula

PTOT is the total power dissipation;

RDS (ON) is the total conduction impedance (HS+LS);

IOUT (RMS) is the effective value of the output current.

The maximum power consumption that the device can withstand depends on the ambient temperature and heat dissipation.

Note: RDS (ON) increases with temperature, so power consumption increases as the device temperature increases.

AT8837 Built-in thermal shutdown protection, when the junction temperature reaches about 160 °C, the H bridge will be shut down until the temperature drops to a safe range.

The chip is easy to touch and turn off because of high power consumption, insufficient heat dissipation or high ambient temperature.

Power and input pins

The VM does not have an undervoltage lockout function (UVLO). As long as the VCC is greater than 2.7V, the internal circuit logic will remain in operation, which means that the VM supply voltage can be as low as 0V, but the load cannot be fully driven in the low VM state.

Regardless of whether the VCC and VM ports are connected to the power supply, the input pins should be configured under recommended operating conditions. There is no leakage current path between the input pins and the power supply. Each input pin has a pull-down resistor (about 100k Ω).

Power supply recommendations

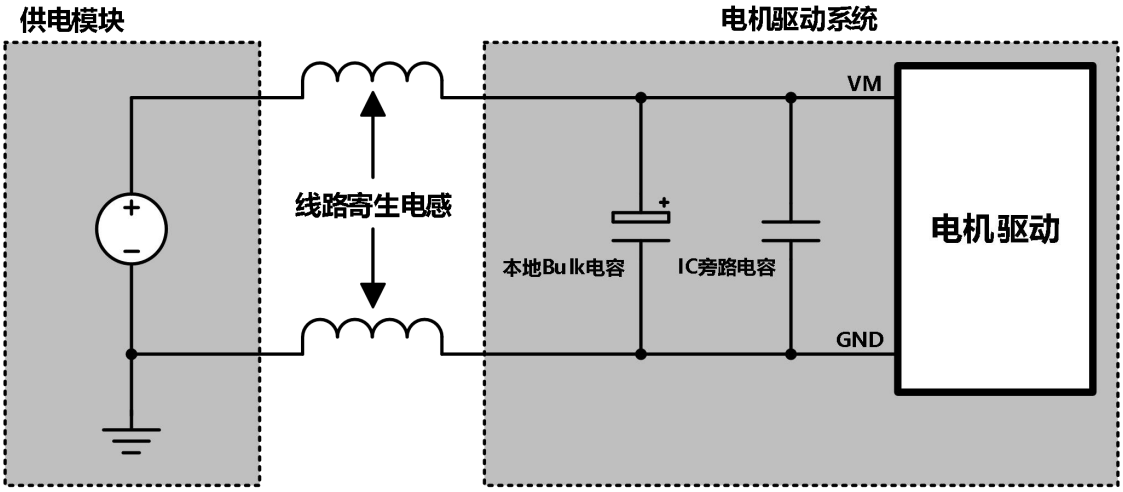
Both the VM and the VCC should be connected to a 0.1uF ceramic capacitor to ground, and the capacitor should be placed as close to the device as possible.

The right Bulk capacitor is the key to motor drive system design. Generally, the larger the Bulk capacitor, the better the effect, but it also brings the cost and PCB size increase.

The capacitance value required depends on the following factors:

Maximum current required by the motor system
The capacitance of the power supply and its ability to supply current
The parasitic inductance between the power supply and the motor system
Acceptable voltage ripple
Type of motor used (brushed, brushless, stepper)
Motor braking method

The inductance between the power supply and the motor system limits the rate of change of output current. If the capacitance value of the local Bulk capacitor is set too low, the system voltage will fluctuate when encountering high currents or sudden changes in motor load; if sufficient Bulk capacitors are used, the voltage can remain stable and provide a large current to the motor.



Example configuration of a motor drive system powered by an external power supply

The voltage rating of bulk capacitor should be slightly higher than the working voltage to prevent the motor from overvoltage to the power supply.

Map layout notes

The PCB should be covered with a large area of copper, and the power and ground lines should have enough width. In order to optimize the electrical characteristics and thermal performance of the circuit, the chip should be directly attached to the PCB, copper covered.

For VM and VCC ports, use a ceramic capacitor with low ESR to connect to ground. The recommended capacitance is 0.1uF. These capacitors should be placed as close as possible to the VM and VCC pins and connected through a wide enough ground wire and GND pin.

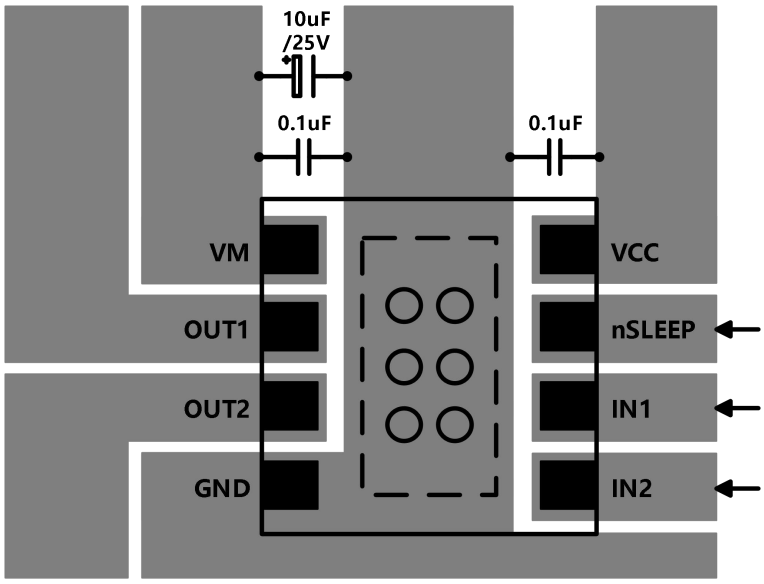
In order to avoid the capacitance coupling problem caused by high speed dV/dt transformation, the output end of the drive circuit and the input end of the logic control are isolated by ground wire.

Ground wire setting

All ground lines in the chip should be connected together, and the connection should be as short as possible. One optimization scheme is to lay the ground lines under the device, in a star pattern.

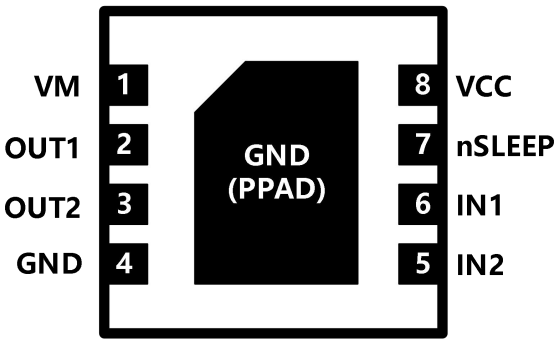
A piece of copper with the right size is placed on the back of the PCB to improve circuit performance.

Map example



Simplified map example

Pin definition



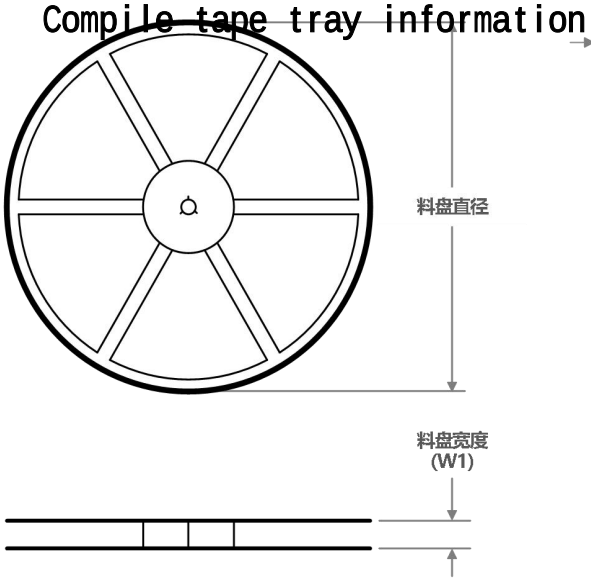
AT8837

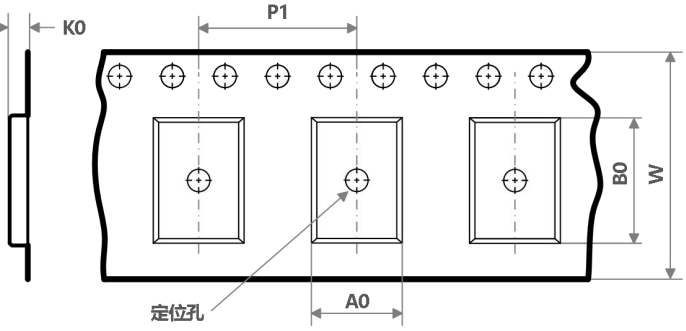
DFN-8

Pin list

Pin name	Pin number	Pin type	Pin description	External components or connections
GND	4	PWR	Chip it	All GND pins and bare pads of the chip should be connected to the power ground.
PPAD	-	PWR		
VM	1	PWR	Motor power supply	Connect an external 0.1uF ceramic capacitor to ground for bypass.
VCC	8	PWR	Logic power supply	Connect an external 0.1uF ceramic capacitor to ground for bypass.
NC	-	-	-	The pins are suspended.
IN1	6	I	Control logic input	
IN2	5	I	Control logic input	
nSLEEP	7	I	Sleep mode input	Logic high level, the chip works normally; logic low level, the chip enters low power sleep mode. Built-in pull-down resistor.
OUT1	2	O	H bridge output 1	Connect to the motor coil.
OUT2	3	O	H bridge output 2	

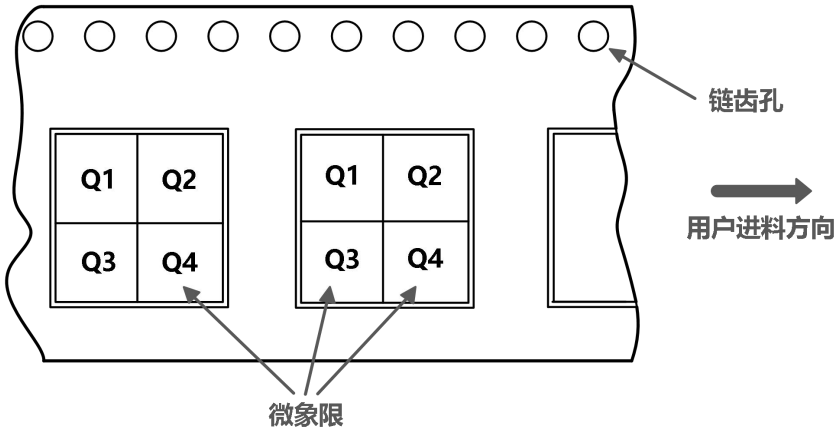
Compile tape tray information





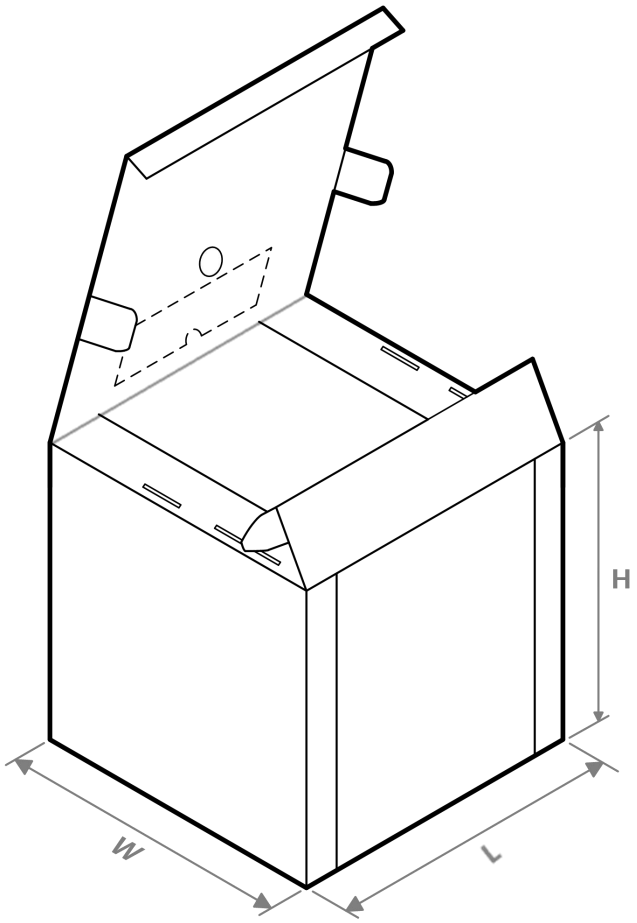
A0	Bin width
B0	Length of trough
K0	Bin thickness
W	Overall width of the carrier
P1	Center spacing of adjacent slots

Bandage PIN 1 Quadrant allocation



Device	Package Type	Package Characteristic	Number of pins	SPQ	Charging tray Diameter (mm)	Charging tray Width (mm)	(mm)	(mm)	(mm)	(mm)	(mm)	Pin 1 Quadrant
AT8837	DFN	-	8	3000	178	8			0.75			Q2

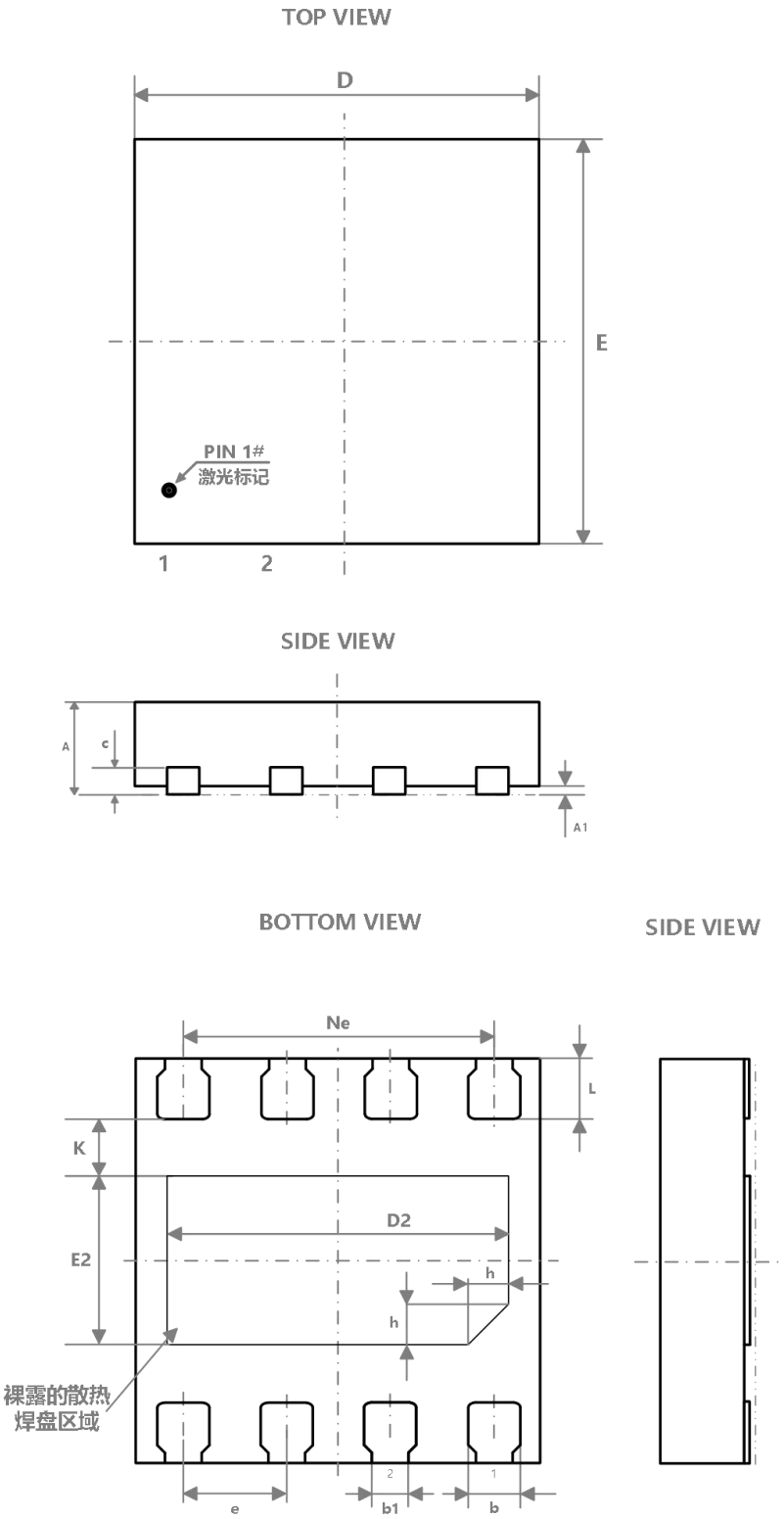
Band material tray packaging size



Device	Packaging type	Packaging identification	Number of pins	SPQ	Length (mm)	Width (mm)	Altitude (mm)
AT8837	DFN	-	8	3000	210	210	210

Package information

DFN-8



Symbol	Millimetre (mm)		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.11	0.16	0.21
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.60	1.70	1.80
e	0.50BSC		
Ne	1.50BSC		
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
L	0.25	0.30	0.35
h	0.15	0.20	0.25
K	0.20	0.25	0.30