description

The HR8825 is an integrated micro-stepper motor driver with built-in stepping tables, providing solutions for printers, scanners, and other automated equipment. It is designed to enable bipolar stepper motors to operate in full, half, 1/4, 1/8, 1/16, and 1/32 step modes. The stepping mode is selected by the logical input MODEx. The output drive capability reaches 38V and ±2.5A. The HR8825's deceleration mode is programmable.

The decoder is a key to the easy implementation of HR8825. A simple STEP input, just one pulse, can make the motor complete a step, eliminating the need for phase sequence tables, high-frequency control lines, and complex programming interfaces. This makes it more suitable for situations where there are no complex microprocessors or when microprocessors are overburdened.

The internal synchronous rectifier control circuit improves the power consumption during PWM operation. The internal protection circuit includes: delayed overheating protection, undervoltage lockout and overcurrent protection. There is no need for special power-up timing.

HR8825 Provides a TSSOP-28 package with exposed pads, which can effectively improve heat dissipation performance and is lead-free. The pin frame is 100% Wuxi electroplating.

Model selection

Model	Package	Pack	Quantity
HR8825	TSSOP28	Piping	30 Slices/ tubes

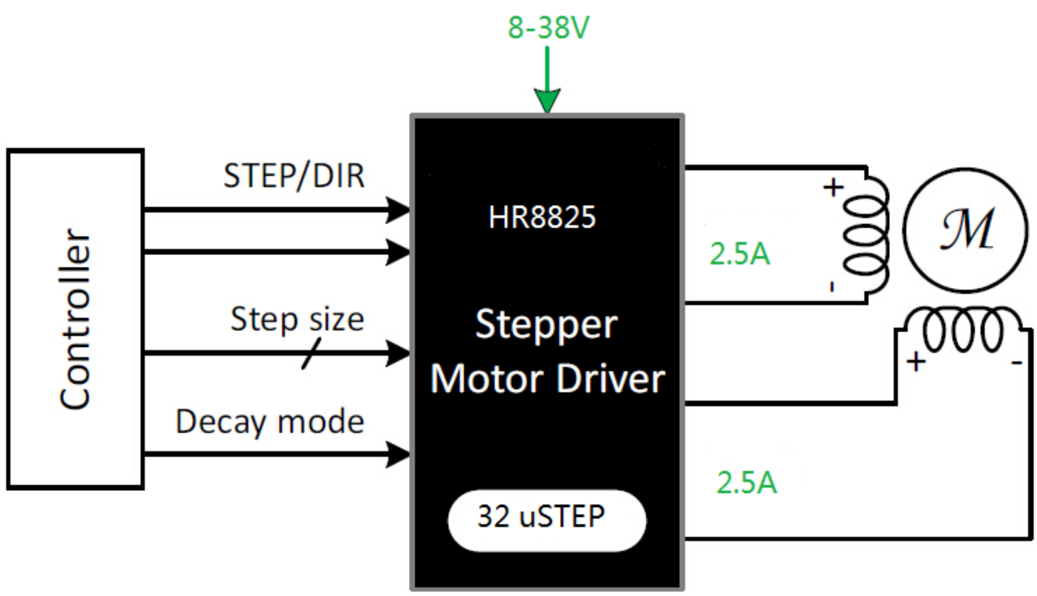
characteristic

Low on-resistance RDS (ON)
Built-in microstep phase sequence meter
Supports hybrid attenuation mode
8V-38V power supply, 2.5A output capacity
Internal under-voltage lockout
overcurrent protection
Overheat shutdown circuit
Built-in 3.3V reference voltage output
Six step modes, up to 32 subdivisions

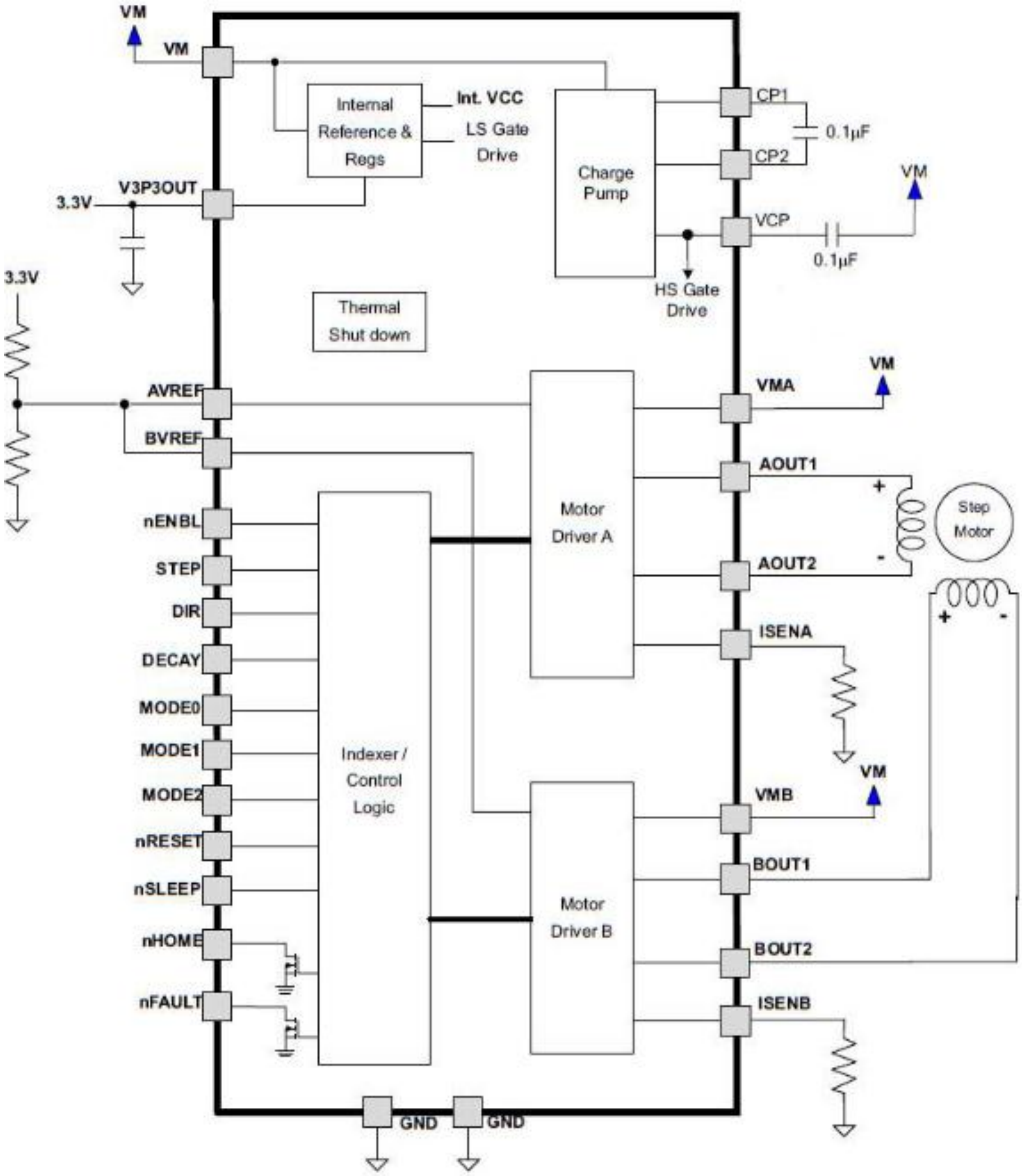
Packaging form

28 lead TSSOP with exposed thermal pad

Simplify the application diagram



functional block diagram



The working limit of the circuit is at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Load Supply Voltage	VM		-0.3 to 40	V
Output Current	I_{OUT}		±2.5	A
Logic Input voltage	V_{IN}		-0.3 to 7	V
Sense Voltage	V_{SENSE}		-0.5 to 0.8	V
Reference Voltage	V_{REF}		-0.3 to 4	V
Operating Ambient Temperature	T_A	Range S	-20 to 85	℃
Maximum Junction	T_J(max)		150	℃
Storage Temperature	T_{stg}		-55 to 150	℃

Recommend working conditions

		MIN	NOM	MAX	UNIT
VM	Motor power supply voltage(1)	8		38	V
VREF	VREF input voltage(2)	1		3.5	V
IV3P3	V3P3OUT load current			1	mA

(1) All VM pins must be connected to the same power supply.

(2) When the voltage on VREF is in the range of 0V to 1V, its working accuracy is not guaranteed.

precautions for use:

1、 Current configuration:

$I_{Trip\ MAX}$ = VREF / (5×Rs),

In the application of high current, in the PCB layout, try to make the path from the ISENx pin to the galvanometer resistance short and thick, and it is recommended to make PCB 2oz copper. If this line is too thin and long, the actual current needs to calculate the resistance of this PCB layout.

In the application of high current, heat dissipation should be fully considered to avoid excessive temperature of the chip.

2、 DECAY Configuration:

DECAY Grounding: the output current rises slowly, the decay is mixed, and the attenuation time is about 25us.

DECAY Suspended: the output current is fully mixed and attenuated, and the attenuation time is about 25us.

Decay time change: In order to adapt to different motor and voltage applications, customers can connect a pull-down resistor outside the DECAY pin according to their own conditions to reduce the decay time. The DECAY built-in pull-down 22k resistor is recommended. The external resistor is between 22k and 100k.

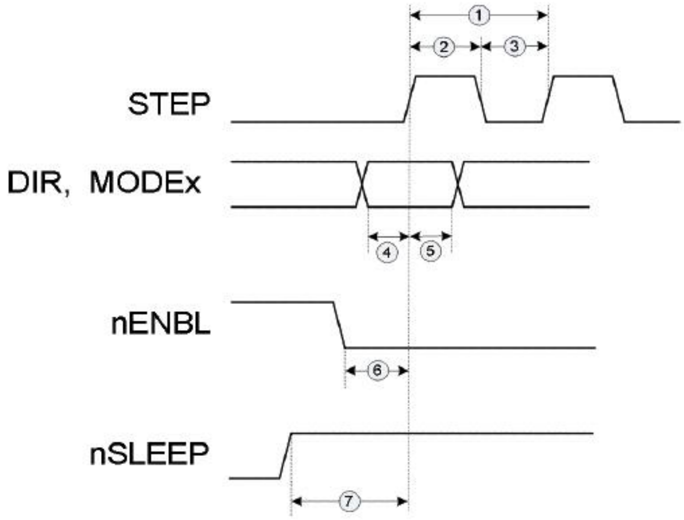
Electrical characteristics at Ta = 25°C, VM=24 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
Power supply	VM	Operating	8		38	V
Power supply under voltage	V_{UVLO}	VM rising		7	7.5	V
Output conduction resistance	$R_{DS(ON)}$	Source Driver, I_{OUT}=-1A		200		mΩ
		Sink Driver, I_{OUT}=1A		200		mΩ
Power supply static current	I_{VM}	f_{PWM} <50 kHz		7	10	mA
		SLEEP		10	20	uA
V3P3OUT REGULATOR						
V3P3, output voltage	V3P3	IOUT = 0 to 1 mA	3.1	3.3	3.5	V
Control Logic						
Logic input level	$V_{IN(1)}$		2		5.25	V
	$V_{IN(0)}$			0.6	0.7	V
Logical input hysteresis	VHYS			0.45		V
Logic input current	$I_{IN(1)}$	V_{IN} = 3.3 V			100	uA
	$I_{IN(0)}$	V_{IN} = 0 V	-20		20	uA
Logic input internal pull-down resistor	RPD	nENBL, nRESET, DIR, STEP, MODEx	-	100	-	KΩ
		nSLEEP	-	1	-	MΩ
nHOME, nFAULT OUTPUTS (OPEN-DRAIN OUTPUTS)						
Output voltage	VOL	IO = 5 mA			0.5	V
Output leakage current	IOH	VO = 3.3 V			1	uA
DECAY						
Decay time	tOFF	Suspended, fully mixed decay		25		us
		External 56k pull-down resistor, full hybrid attenuation		18		us
		Ground, the current rises slowly and decays, and the decrease is mixed		25		us
Internal pull-down resistor	RPD			22		KΩ
MOTOR DRIVER						
	fPWM					KHz

Internal PWM frequency				50		
Blanking time	tBLANK			1.75		us
Rise time	tR		70		200	ns
Drop-out time	tF		60		180	ns
Dead zone time	tDEAD			400		ns
Protection						
Overcurrent threshold	I_{OCPST}		3.8		4.5	A
Over temperature threshold	T_{TSD}		150	160	180	℃
Overtemperature lag	T_{TSDHYS}			15		℃
CURRENT CONTROL						
xVREF input current	IREF	xVREF = 3.3 V	-3		3	uA
xISENSE trip voltage	VTRIP	xVREF = 3.3 V, 100% current setting	635	660	685	mV
Current trip accuracy (relative to programmed value)	ΔITRIP	xVREF = 3.3 V , 5% current setting	-20		20	%
		xVREF = 3.3 V , 10% - 34% current setting	-15		15	
		xVREF = 3.3 V , 38% - 67% current setting	-10		10	
		xVREF = 3.3 V , 71% - 100% current	-5		5	

Current sense amplifier gain	AISENSE	Reference only		5		V/V

Requirements on the timing of circuit control signals:



			MIN	MAX	UNIT
1	fSTEP	Step frequency		250	KHz
2	tWH(STEP)	Pulse duration, STEP high	1.9		us
3	tWL(STEP)	Pulse duration, STEP low	1.9		us
4	tSU(STEP)	Setup time, command to STEP rising	200		ns
5	tH(STEP)	Hold time, command to STEP rising	200		ns
6	tENBL	Enable time, nENBL active to STEP	200		ns
7	tWAKE	Wakeup time, nSLEEP inactive to STEP	1		ms

Microstep true value table

MODE2	MODE1	MODE0	Microstep Resolution
0	0	0	Synchronizing
0	0	1	2. Segmentation
0	1	0	Four segments
0	1	1	Eight segments
1	0	0	16 sub-categories
1	0	1	32 subdivision
1	1	0	
1	1	1	

Module function description

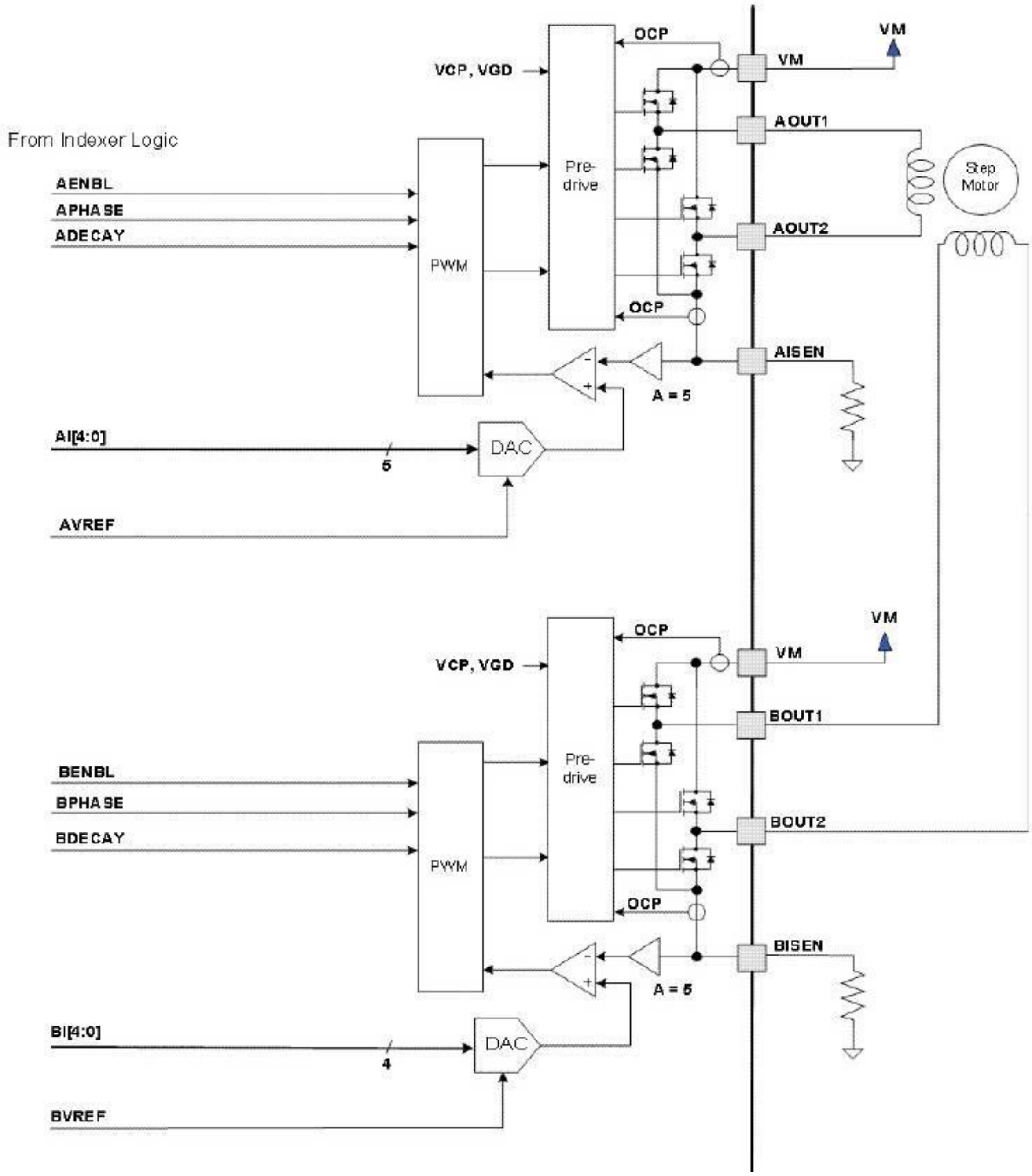
HR8825 Bipolar stepper motor provides integrated drive solution, built-in two NMOS H bridge, current detection and rectifier circuit, micro-stepper phase sequence meter. HR8825 Power supply range from 8V to 38, providing maximum current output of 2.5A.

The simple STEP/DIR interface simplifies the control circuit, and the built-in microstepping phase table enables high subdivision mode. Current rectification is programmable to enable mixed attenuation mode.

The low-power sleep mode allows the system to save power when the motor is not needed.

PWM Motor Drivers

HR8825, which includes two H-bridge motor drive circuits using PWM current control. The following figure shows the functional modules of the circuit:



Note: There are multiple VM pins on the chip. All VM pins need to be connected together and connected to the power supply.

Current Regulation

Through a fixed-frequency PWM current rectifier, the current flowing through the motor drive bridge arms is limited or controlled. When an H-bridge is enabled, the current flowing through the corresponding arm rises at a slope determined by the DC voltage VM and the inductive characteristics of the motor. When the current reaches a set threshold, the driver turns off this current until the next PWM cycle begins.

During the stepping process, the current rectifier circuit causes the current flowing through the two bridge arms to vary in a quasi-sinusoidal manner, allowing the motor to rotate smoothly. The PWM target current is determined by dividing the voltage across the current sensing resistor connected to the xISEN pin by a divisor factor (5) and a reference voltage. The reference voltage is the input voltage on the xVREF pin.

The 100% chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}}$$

For example, if a 0.5Ω resistor is used and the voltage on the xVREF is 3.3V, then the 100% chopped current is 1.32A.

The reference voltage is measured by the internal DAC, so that the micro subdivision of the stepper motor can be achieved.

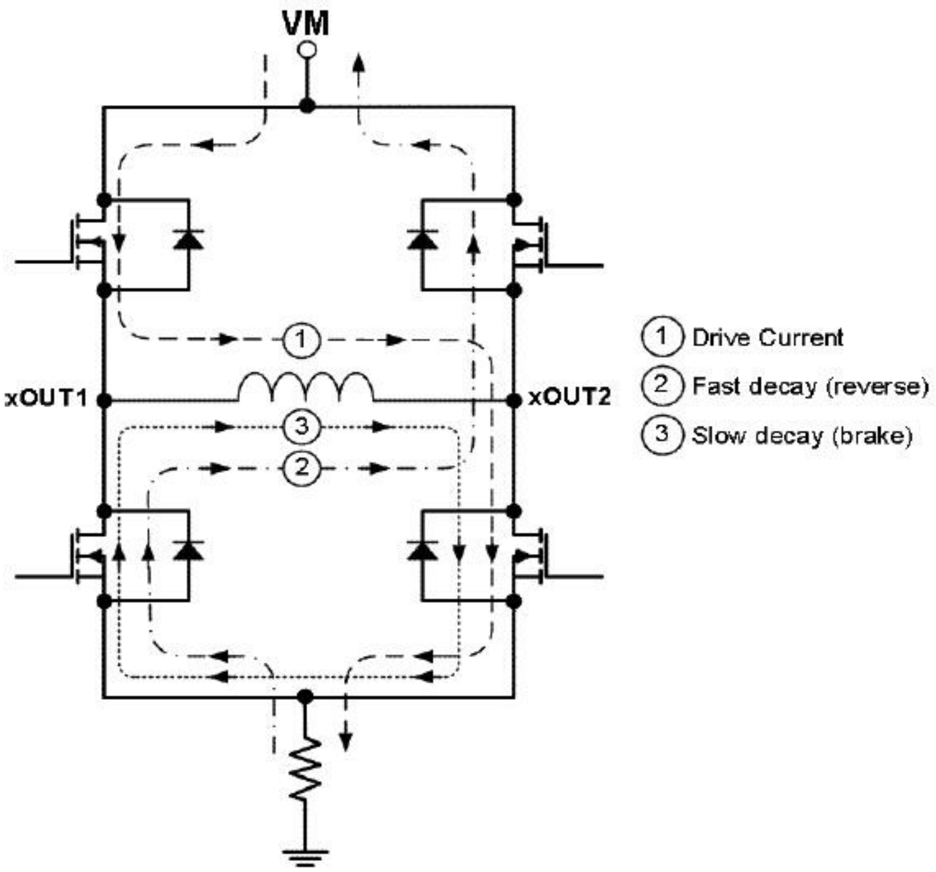
Decay Modes

During PWM current rectification, the H-bridge is enabled so that the current driving through the motor bridge arms is until the PWM chopping current threshold is reached. The current path is described in example 1 below. The direction of the current described in the figure is defined as forward.

Once the PWM chopping current threshold is reached, the H bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current threshold is reached, the H bridge reverses the output state, causing the arm current to flow in the opposite direction. When the arm current approaches 0, the H bridge is disabled to prevent reverse current flow. The fast decay current path is shown in example 2 below.

In the slow attenuation mode, the bridge arm current is continued by enabling two low-voltage side FETs. The following figure example 3 shows the slow attenuation current path.



evanescent mode

HR8825 supports hybrid attenuation, which can be determined by the input state of the DECAY: if the DECAY is grounded, it selects slow rise current attenuation; if it is left floating or connected to a high level, it selects full hybrid attenuation. The DEACY pin has an internal 22KΩ pull-down resistor. Therefore, when the DECAY pin is open or not in use, the default attenuation mode is full hybrid attenuation.

In the mixed attenuation mode, fast attenuation begins and is followed by a fixed off time (33% of the PWM cycle) before slow attenuation is turned on until the end of the PWM cycle.

Blanking Time

At the moment when the current is enabled, the voltage on the xISEN pin is ignored, and after a fixed time, the current detection circuit is enabled. This blanking time is usually fixed at 1.75us. This blanking time also determines the minimum PWM time for operating the current decay.

nRESET, nENBLE and nSLEEP Operation

nRESET When the pin is input at low level, the chip resets the internal logic and resets the microstepping phase table to HOME state. At the same time, H bridge is disabled and the logical input on STEP is ignored.

The nENBL pin is used to control the output and enable/disable microstepping phase sequence table operations. When the nENBL input is at a low level, the H bridge outputs enable, and the rising edge of STEP is recognized. When the nENBL input is at a high level, the H bridge is disabled, the output is in a high-impedance state, and the STEP input is ignored.

When the pin input is at a low level, the device enters sleep mode, significantly reducing idle power consumption. Once in sleep mode, the H-bridge is disabled, the charge pump circuit stops working, and the V3P3 output is blocked. All internal clocks also cease operation, and all logic inputs are ignored. When the input flips to a high level, the system returns to normal operation and presets the device's output to the HOME state. To ensure the internal charge pump resumes stable operation, the STEP signal only becomes active after SLEEP returns to a high level and a delay of 1 ms.

nRESET and nENABLE have built-in 100KΩ pull-down resistors, and nSLEEP has built-in 1MΩ pull-down resistors.

Protection Circuits

HR8825 Overcurrent protection, overtemperature protection and undervoltage protection.

Overcurrent Protection (OCP)

There is an analog current limiting circuit on each FET, which limits the current flowing through the FET to limit the gate drive. If this overcurrent analog current is maintained for longer than the OCP pulse time, all FETs in the H bridge are disabled and the nFAULT pin outputs a low level.

The overcurrent conditions on the upper and lower arms of the H bridge are independently detected. Ground short, VM short, and short between output will cause an overcurrent shutdown. Note that the overcurrent protection does not use a current detection circuit with PWM current control, so the overcurrent protection function does not affect the xISEN resistor.

Thermal Shutdown (TSD)

If the junction temperature exceeds the safety limit threshold, the H bridge function FET is disabled and the nFAULT pin outputs a low level. Once the junction temperature drops to a safe level, all operations will automatically return to normal.

Undervoltage Lockout (UVLO)

At any time, if the voltage on the VM pin drops below the under-voltage lock threshold, all internal circuits are disabled and all internal resets. When the voltage on the VM rises above the UVLO, all functions automatically resume.

Information on circuit applications

Map notes: A large heat sink should be placed on the PCB board, and a wide ground wire should be connected to the ground line. In order to optimize the electrical characteristics and thermal performance of the circuit, the chip should be directly attached to the heat sink.

For the motor power supply VM, an electrolytic capacitor of no less than 100uF should be connected to the ground coupling, and the capacitor should be placed as close as possible to the device.

In order to avoid the capacitance coupling problem caused by high speed dv/dt transformation, the wiring at the output end of the drive circuit should be far away from the wiring at the logic control input end. The lead wire at the logic control end should be low impedance to reduce the noise caused by thermal resistance.

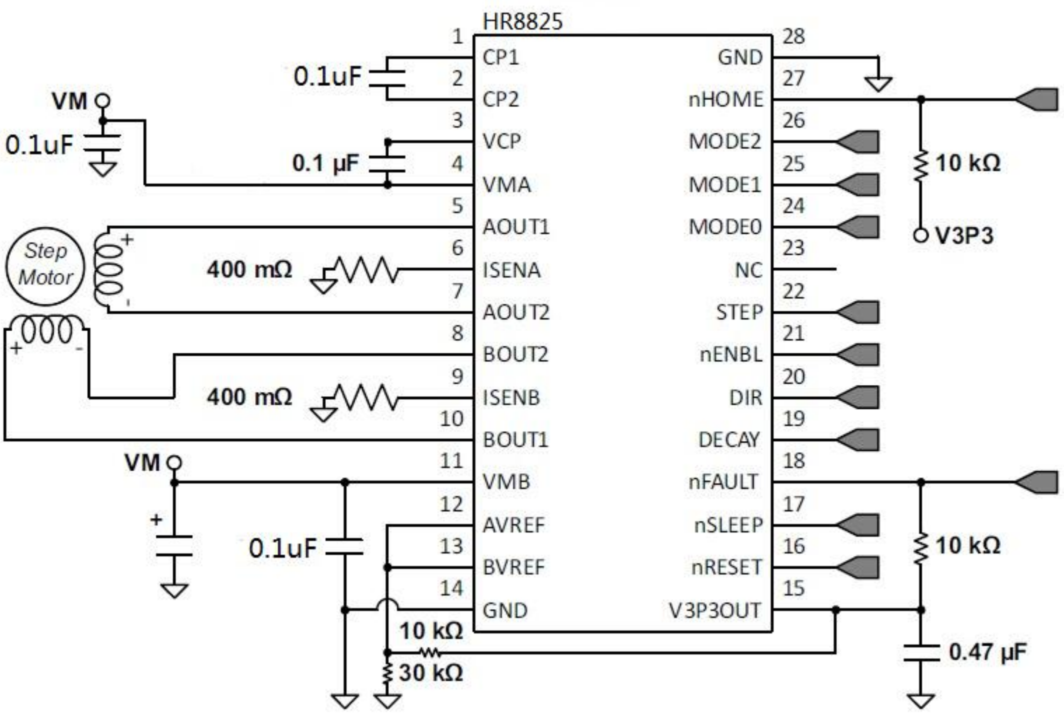
Ground wire Settings: The connection between AGND and PGND must be shorted outside the chip. All ground wires should be connected together, and the connections should be as short as possible. A star-diffused ground wire layout located under the device will be an optimized design.

Adding a copper heat sink under the laid ground will better optimize circuit performance.

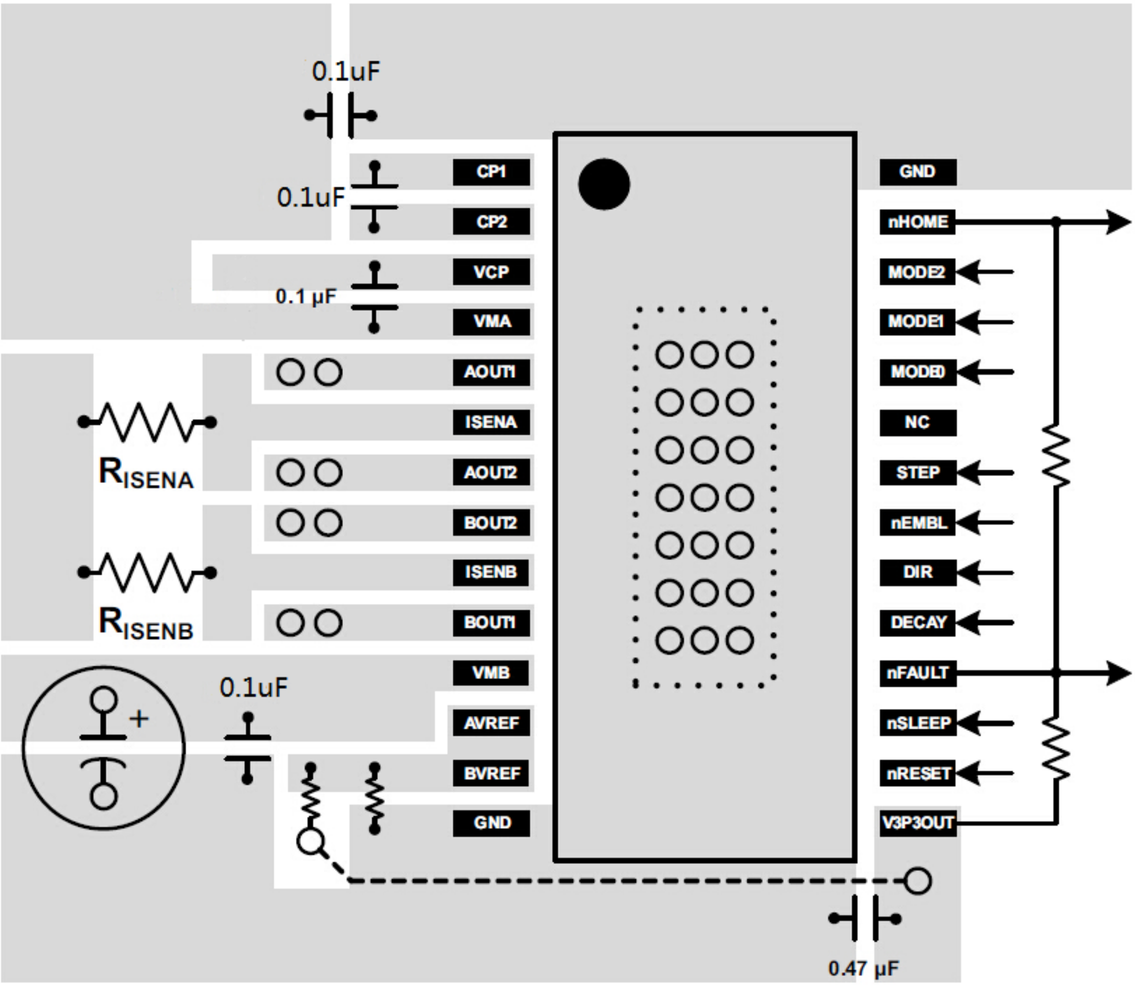
Current Sampling Settings: To reduce errors caused by parasitic resistance on the ground wire, the sampling resistor RS for motor current should be set separately from the ground wire that is grounded, minimizing errors caused by other factors. The separate ground wire should ultimately be connected to a star-distributed ground busbar, with the connection being as short as possible. For small-value Rs, since the voltage drop V=I * Rs is less than 0.5V, the voltage drop on the PCB traces will be significant compared to 0.5V, which must be taken into account.

PCB should avoid using test transfer sockets as much as possible. The connection resistance of test sockets may change the size of Rs and cause errors to the circuit. The selection of Rs value follows the following formula:

$$Rs = 0.5/I_{TRIP\ max}$$



Typical application schematic



Typical reference layout

Microstep phase sequence table

Home microstep position at Step Angle 45°; DIR = H

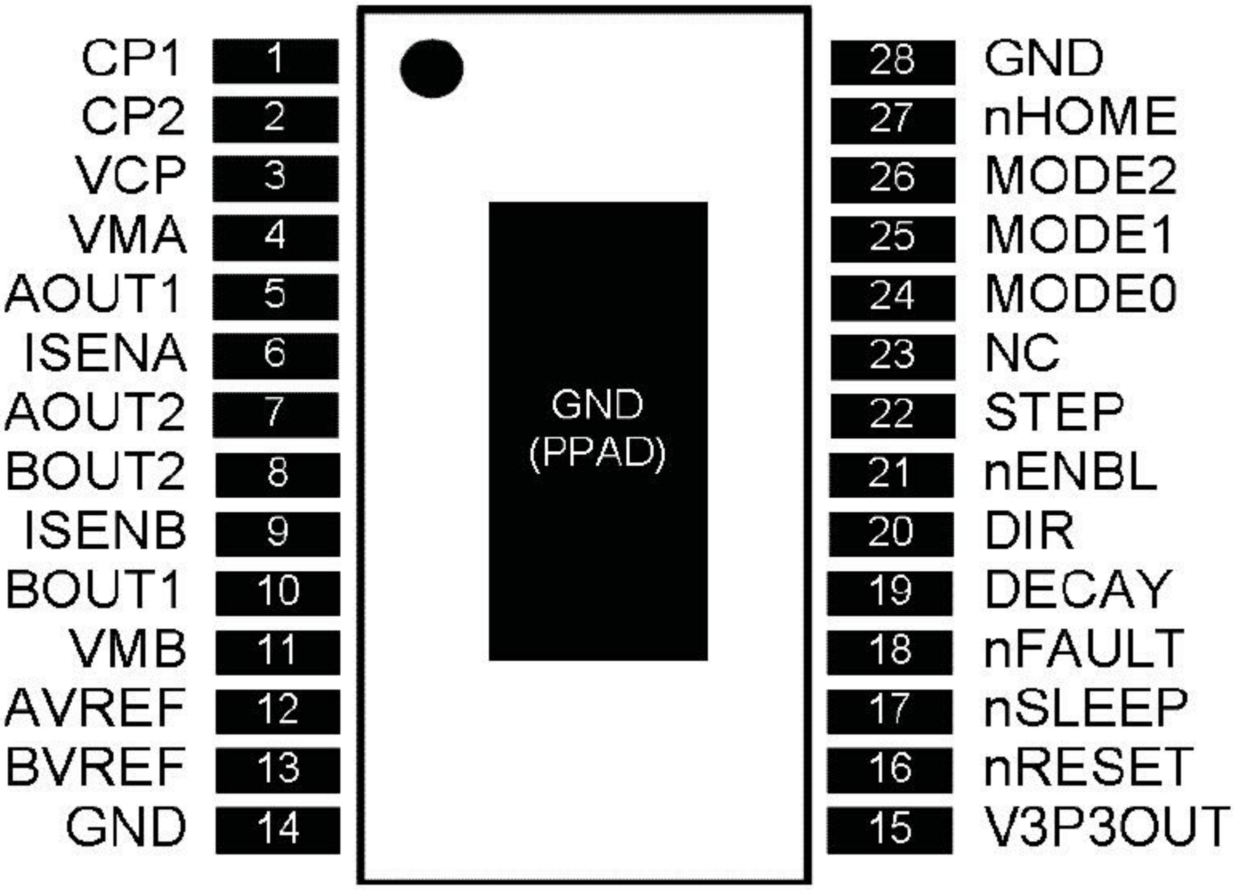
1/32	1/16	1/8	1/4	1/2	full	Current A(%)	Current B(%)	Step Angle(°)
1	1	1	1	1		100.0	0.0	0.00
2						99.9	4.9	2.81
3	2					99.5	9.8	5.63
4						98.9	14.7	8.44
5	3	2				98.1	19.5	11.25
6						97.0	24.3	14.06
7	4					95.7	29.0	16.88
8						94.2	33.7	19.69
9	5	3	2			92.4	38.3	22.50
10						90.4	42.8	25.31
11	6					88.2	47.1	28.13
12						85.8	51.4	30.94
13	7	4				83.1	55.6	33.75
14						80.3	59.6	36.56
15	8					77.3	63.4	39.38
16						74.1	67.2	42.19
17	9	5	3	2	1	70.7	70.7	45.00
18						67.2	74.1	47.81
19	10					63.4	77.3	50.63
20						59.6	80.3	53.44
21	11	6				55.6	83.1	56.25
22						51.4	85.8	59.06
23	12					47.1	88.2	61.88
24						42.8	90.4	64.69
25	13	7	4			38.3	92.4	67.50
26						33.7	94.2	70.31
27	14					29.0	95.7	73.13
28						24.3	97.0	75.94
29	15	8				19.5	98.1	78.75
30						14.7	98.9	81.56
31	16					9.8	99.5	84.38
32						4.9	99.9	87.19
33	17	9	5	3		0.0	100.0	90.00
34						-4.9	99.9	92.81
35	18					-9.8	99.5	95.63
36						-14.7	98.9	98.44
37	19	10				-19.5	98.1	101.25
38						-24.3	97.0	104.06
39	20					-29.0	95.7	106.88
40						-33.7	94.2	109.69

41	21	11	6			-38.3	92.4	112.50
42						-42.8	90.4	115.31
43	22					-47.1	88.2	118.13
44						-51.4	85.8	120.94
45	23	12				-55.6	83.1	123.75
46						-59.6	80.3	126.56
47	24					-63.4	77.3	129.38
48						-67.2	74.1	132.19
49	25	13	7	4	2	-70.7	70.7	135.00
50						-74.1	67.2	137.81
51	26					-77.3	63.4	140.63
52						-80.3	59.6	143.44
53	27	14				-83.1	55.6	146.25
54						-85.8	51.4	149.06
55	28					-88.2	47.1	151.88
56						-90.4	42.8	154.69
57	29	15	8			-92.4	38.3	157.50
58						-94.2	33.7	160.31
59	30					-95.7	29.0	163.13
60						-97.0	24.3	165.94
61	31	16				-98.1	19.5	168.75
62						-98.9	14.7	171.56
63	32					-99.5	9.8	174.38
64						-99.9	4.9	177.19
65	33	17	9	5		-100.0	0.0	180.00
66						-99.9	-4.9	182.81
67	34					-99.5	-9.8	185.63
68						-98.9	-14.7	188.44
69	35	18				-98.1	-19.5	191.25
70						-97.0	-24.3	194.06
71	36					-95.7	-29.0	196.88
72						-94.2	-33.7	199.69
73	37	19	10			-92.4	-38.3	202.50
74						-90.4	-42.8	205.31
75	38					-88.2	-47.1	208.13
76						-85.8	-51.4	210.94
77	39	20				-83.1	-55.6	213.75
78						-80.3	-59.6	216.56
79	40					-77.3	-63.4	219.38
80						-74.1	-67.2	222.19
81	41	21	11	6	3	-70.7	-70.7	225.00
82						-67.2	-74.1	227.81
83	42					-63.4	-77.3	230.63
84						-59.6	-80.3	233.44

85	43	22				-55.6	-83.1	236.25
86						-51.4	-85.8	239.06
87	44					-47.1	-88.2	241.88
88						-42.8	-90.4	244.69
89	45	23	12			-38.3	-92.4	247.50
90						-33.7	-94.2	250.31
91	46					-29.0	-95.7	253.13
92						-24.3	-97.0	255.94
93	47	24				-19.5	-98.1	258.75
94						-14.7	-98.9	261.56
95	48					-9.8	-99.5	264.38
96						-4.9	-99.9	267.19
97	49	25	13	7		0.0	-100.0	270.00
98						4.9	-99.9	272.81
99	50					9.8	-99.5	275.63
100						14.7	-98.9	278.44
101	51	26				19.5	-98.1	281.25
102						24.3	-97.0	284.06
103	52					29.0	-95.7	286.88
104						33.7	-94.2	289.69
105	53	27	14			38.3	-92.4	292.50
106						42.8	-90.4	295.31
107	54					47.1	-88.2	298.13
108						51.4	-85.8	300.94
109	55	28				55.6	-83.1	303.75
110						59.6	-80.3	306.56
111	56					63.4	-77.3	309.38
112						67.2	-74.1	312.19
113	57	29	15	8	4	70.7	-70.7	315.00
114						74.1	-67.2	317.81
115	58					77.3	-63.4	320.63
116						80.3	-59.6	323.44
117	59	30				83.1	-55.6	326.25
118						85.8	-51.4	329.06
119	60					88.2	-47.1	331.88
120						90.4	-42.8	334.69
121	61	31	16			92.4	-38.3	337.50
122						94.2	-33.7	340.31
123	62					95.7	-29.0	343.13
124						97.0	-24.3	345.94
125	63	32				98.1	-19.5	348.75
126						98.9	-14.7	351.56
127	64					99.5	-9.8	354.38
128						99.9	-4.9	357.19

Pin-out Diagram

Top View

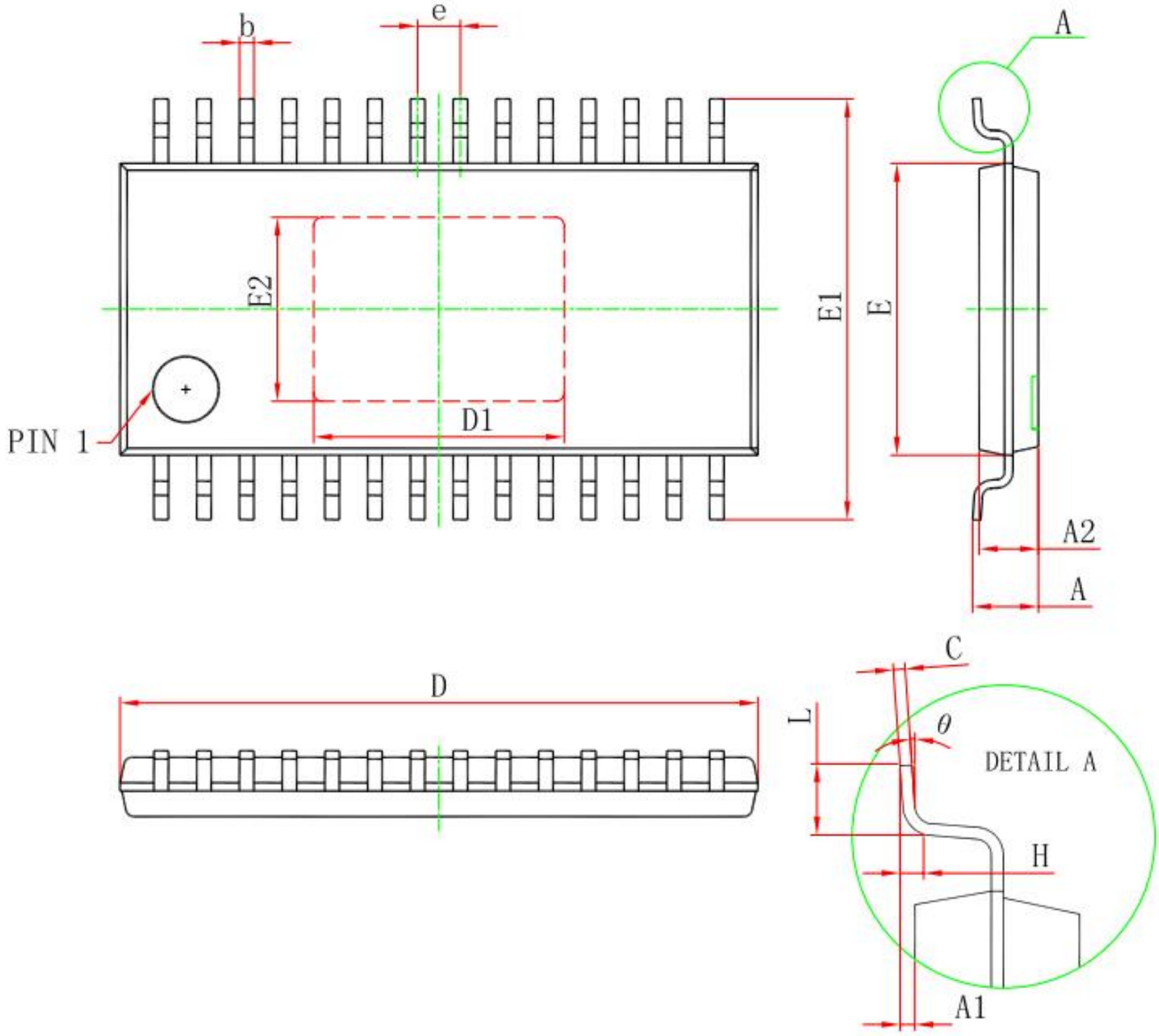


Terminal List Table

NAME	PIN	Pin Description	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND			
GND	14、28	Chip ground	All GND pins and the bottom heat sink must be grounded
PPAD	-		
VMA	4	A H bridge power supply	All VM pins are connected together and power filtering is done
VMB	11	B H bridge power supply	
V3P3OUT	15	3.3V rectified ou-tput	Connect 0.47uF capacitor to ground
CP1	1	Charge pump	Connect 0.1uF capacitor between the two
CP2	2		
VCP	3	High-end gate grid drive	Connect the 0.1uF capacitor to VM
CONTROL			
nENBL	21	Enable input	Logic high level turns off the output; logic low level enables the output; internal pull-down 100k.
nSLEEP	17	Hibernation input	Logic high enables the output; logic low puts the chip into sleep mode; internal pull-down 1M.
STEP	22	Stepping clock in-put	The upward rise moves the internal timing forward; the internal pull-down is 100k
DIR	20	Direction control input	Direction control input; built-in pull-down 100k
MODE0	24	Split input 0	Subdivision mode input-full, 1/2,1/4,1/8/,1/16,1/32 built-in dropdown 100k.
MODE1	25	Split input 1	
MODE2	26	Split input 2	
DECAY	19	Input attenuation mode	The ground selection current rises slowly and declines in mixed decay; the suspension selection is fully mixed decay; the attenuation time can be adjusted by an external pull-down resistor; the built-in pull-down 22k
nRESET	16	Reset input	Logic low enables the chip; logic high resets the chip; built-in pull down 100k
AVREF	12	H bridge reference voltage input	Reference voltage input, usually two pins are connected to V3P3OUT, it is recommended to add 0.1uF capacitor to ground for filtering
BVREF	13	B H bridge refere-nce voltage input	
NC	23	Hang in the air	Not defined
STATUS			
nFAULT	18	Fault output	When an anomaly occurs, the output is low, and the open leakage output is enabled, so the external needs to be pulled up (over temperature, over current)
nHOME	27	Home output	The output of the HOME state is low, and the open drain output is

			enabled to pull up externally
OUTPUT			
ISENA	6	Bridge A Isense	Connect the receiving current resistance to ground
ISENB	9	Bridge B Isense	Connect the receiving current resistance to ground
AOUT1	5	Bridge A output 1	Connect to motor winding A Positive current is AOUT1 → AOUT2
AOUT2	7	Bridge A output 2	
BOUT1	10	Bridge B output 1	Connect to motor winding B Positive current is BOUT1 → BOUT2
BOUT2	8	Bridge B output 2	

TSSOP 28 with exposed thermal pad



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	9.600	9.800	0.378	0.386
D1	3.710	3.910	0.146	0.154
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.700	2.900	0.106	0.122
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

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