**SIT1040Q**

Corel 5V power supply, ±40V interface withstand voltage, 1 Mbps high-speed CAN bus transceiver

## characteristic:

- Fully compatible with the "ISO 11898" standard;
- Comply with AEC-Q100 requirements;
- Built-in over temperature protection;
- Overcurrent protection function;
- Visible timeout function;
- Low current standby mode with bus wake-up function (typical value 5μA);
- The unpowered node does not interfere with the bus;
- At least allow 110 nodes to connect to the bus;
- High speed CAN, transmission rate can reach 1 Mbps;
- High electromagnetic interference resistance;
- Provide HVSON8 / DFN3*3-8, small form factor, pinless package.

## Typical product appearance:

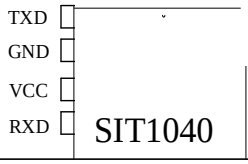

Provide green and lead-free packaging

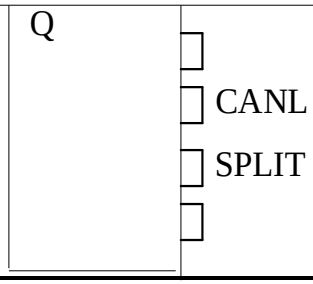
## description

SIT1040Q is an interface chip applied between CAN protocol controller and physical bus. It can be used in truck, bus, car, industrial control and other fields. The rate can reach 1Mbps, and it has the ability to transmit differential signal between bus and CAN protocol controller.

| Parameter | Symbol | Test condition | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| Service voltage | $V_{cc}$ | | 4.75 | 5.25 | V |
| Peak transfer rate | $1/t_{bit}$ | Non-zero code | 1 | | Mbaud |
| CANH、CANL Input and output voltage | $V_{can}$ | | -40 | +40 | V |
| Total line differential voltage | $V_{diff}$ | | 1.5 | 3.0 | V |
| Ambient temperature | $T_{amb}$ | | -40 | 125 | ℃ |
| ESD ability | $V_{esd}$ | Human model (HBM) | ±8 | | KV |

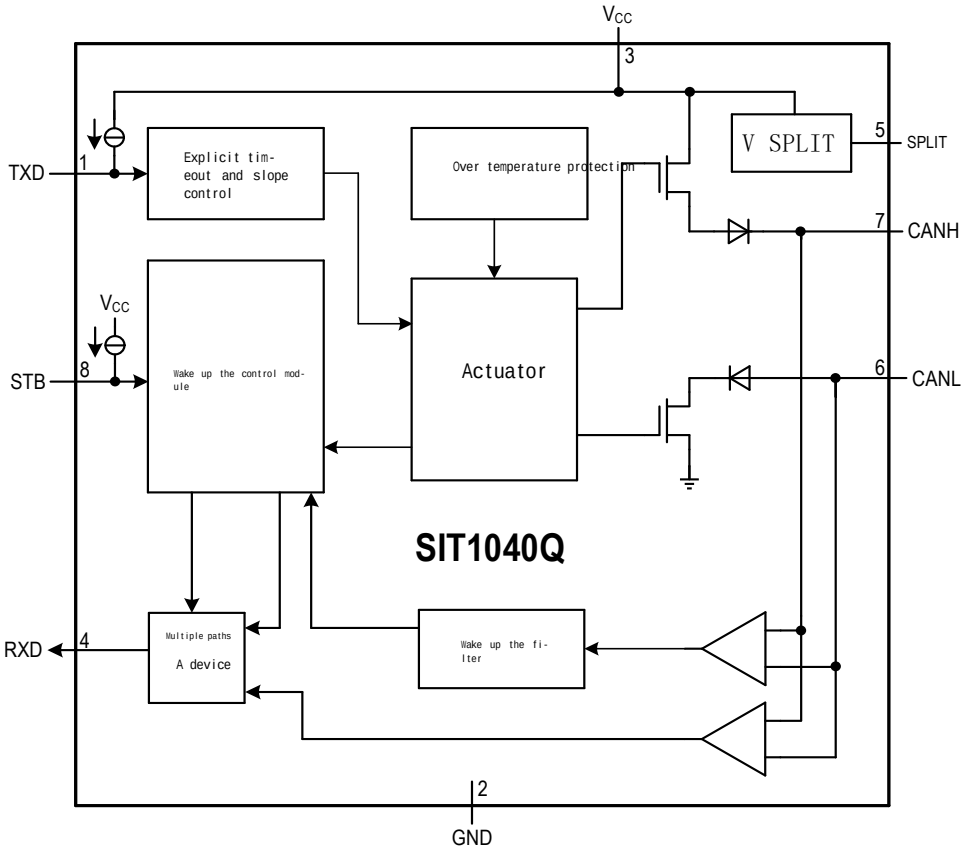
## Pin distribution diagram




Q
CANL
SPLIT

| Pin number | Pin name | Pin function |
|---|---|---|
| 1 | TXD | Data input end of transmitter |
| 2 | GND | The earth |
| 3 | VCC | Power Supply Voltage |
| 4 | RXD | Receiver data output end |
| 5 | SPLIT | Common mode stable output |
| 6 | CANL | Low potential CAN voltage input/output terminals |
| 7 | CANH | High potential CAN voltage input/output terminal |
| 8 | STB | High speed and standby mode selection, low level is high speed |

Note: DFN3*3-8/HVSON8 package, the back pad is connected to the GDN pin of the chip. If better heat dissipation performance is required, the back pad can be connected to the appropriate "ground" of the PCB board.




SIT1040Q Internal block diagram

## absolute rating

| Parameter | Symbol | Big or small | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | -0.3~+6 | V |
| MCU, side port | TXD, RXD, STB | -0.3~VCC+0.3 | V |
| Total line-side port voltage | CANL, CANH, SPLIT | -40~40 | V |
| 6, The transient voltage of pin 7 is shown in Figure 7 | $V_{tr}$ | -200~+200 | V |
| Storage operating temperature range | | -55~150 | ℃ |
| Ambient temperature | | -40~125 | ℃ |
| Welding temperature range | | 300 | ℃ |

The maximum limit parameter value is the value beyond which the device may suffer irrecoverable damage. Under these conditions, it is not conducive to the normal operation of the device. Continuous operation of the device at the maximum allowable rating may affect the reliability of the device. All voltage reference points are ground.

## DC characteristics of the total signal transmitter

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| CANH output voltage (visible) | $V_{OH(D)}$ | VI=0V, STB=0V, RL=60Ω, Figure 1 and Figure 2 | 2.9 | 3.4 | 4.5 | V |
| CANL Output Voltage (Visible) | $V_{OL(D)}$ | | 0.8 | | 1.5 | V |
| Total output voltage (latent) | $V_{O(R)}$ | VI=3V, STB=0V, RL=60Ω, Figure 1 and Figure 2 | 2 | 2.5 | 3 | V |
| The total signal output is a differential voltage (dominance) | $V_{OD(D)}$ | VI=0V, STB=0V, RL=60Ω, Figure 1 and Figure 2 | 1.5 | | 3 | V |
| Total line differential output voltage (covert gender) | $V_{OD(R)}$ | VI=3V, S=0V, Figure 1, Figure 2 | -0.012 | | 0.012 | V |
| | | VI=3V, STB=0V, NO LOAD | -0. 5 | | 0.05 | V |
| Output voltage symmetry | $V_{TXsym}$ | $V_{TXsym}= V_{CANH} + V_{CANL}$ | $0.9V_{CC}$ | | $1.1V_{CC}$ | V |
| Common-mode output voltage | $V_{OC}$ | STB=0V, graph 8 | 2 | 2.5 | 3 | V |
| The difference | $\triangle V_{OC}$ | | | 30 | | mV |

| | | | | | | |
|---|---|---|---|---|---|---|
| between the dominant and recessive common mode output voltages | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Short circuit output current | $I_{OS}$ | CANH=-12V, CANL=open, graph 11 | -105 | -40 | | mA |
| | | CANH=12V, CANL=open, graph 11 | | 0.36 | 1 | |
| | | CANL=-12V, CANH=open, graph 11 | -1 | 0.5 | | |
| | | CANL=12V, CANH=open, graph 11 | | 40 | 105 | |
| Hidden output current | $I_{O(R)}$ | -27V<CANH<32V 0<VCC<5.25V | -2.0 | | 2.5 | mA |

(If no other description is given, VCC=5V±5%, Temp=TMIN~TMAX, typical value in VCC=+5V, Temp = 25 )

## General transmitter switch characteristics

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| Propagation delay (low to high) | tPLH | STB=0V, graph 4 | 25 | 90 | 150 | ns |
| Propagation delay (high to low) | tPHL | | 20 | 45 | 90 | ns |
| Differential output rise time | tr | | | 80 | | ns |
| Differential output delay time | tf | | | 50 | | ns |
| From the listening mode to the explicit enable time | $t_{EN}$ | Graph 7 | | | 10 | μs |
| Visible timeout time | $t_{dom}$ | Graph 10 | 300 | 450 | 700 | μs |
| Total sleep wake time | $t_{BUS}$ | | 0.7 | | 5 | μs |

(If no other description is given, VCC= 5V±5%, Temp = TMIN~TMAX, typical value is VCC = +5V, Temp = 25 )

## DC characteristics of the total signal receiver

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| Enter the threshold | $V_{IT+}$ | STB=0V, graph 5 | | 750 | 900 | mV |
| Negative input threshold | $V_{IT-}$ | | 500 | 650 | | |
| Comparator thres- | $V_{HYS}$ | | 80 | 100 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| hold hysteresis interval | | | | | | |
| High level output voltage | $V_{OH}$ | IO=-2mA, graph 6 | 4 | 4.6 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| Low level output voltage | $V_{OL}$ | IO=2mA, graph 6 | | 0.2 | 0.4 | V |
| Bus input current drops when power is lost | $I_{(OFF)}$ | CANH or CANL=5V, Other pin=0V | | | 5 | μA |
| CANH and CANL are input capacitors to the ground | $C_I$ | | | 18 | | pF |
| CANH, CANL differential input capacitors | $C_{ID}$ | | | 10 | | pF |
| CANH, CANL, input resistance | $R_{IN}$ | TXD=3V, STB=0V | 15 | 32 | 45 | KΩ |
| CANH, CANL differential input resistance | $R_{ID}$ | | 30 | | 90 | KΩ |
| RI (CANH) and RIN (CANL) mismatch | $RI_{match}$ | CANH=CANL | -3% | | 3% | |
| Common-mode voltage range | $V_{COM}$ | | -12 | | 12 | V |

(If no other description is given, VCC=5V±5%, Temp=TMIN~TMAX, typical value in VCC=+5V, Temp = 25 )

## Total line receiver switch characteristics

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| Propagation delay (low to high) | tPLH | STB=0VorVCC, graph 6 | 60 | 100 | 140 | ns |
| Propagation delay (high to low) | tPHL | | 45 | 70 | 100 | ns |
| RXD signal rise time | tr | | | 8 | | ns |
| RXD signal fall time | tf | | | 8 | | ns |

(If no other description is given, VCC=5V±5%, Temp=TMIN~TMAX, typical value in VCC=+5V, Temp = 25 )

## Device switching characteristics

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| Loop delay 1, driver input to receiver output, implicit to explicit | Td(LOOP1) | STB=0V, graph 9 | 90 | | 230 | ns |
| Loop delay 2, driver input to re- | Td(LOOP2) | | 90 | | 230 | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| ceiver output, explicit to impl-icit | | | | | | |

(If no other description is given, VCC=5V±5%, Temp=TMIN~TMAX, typical value in VCC=+5V, Temp = 25 )

## Over temperature protection

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| Overtemperature shutdown | Tj(sd) | | | 160 | | ℃ |

## TXD pin characteristics

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| TXD port high level input current | $I_{IH}$(TXD) | VI=VCC | -2 | | 2 | μA |
| TXD port low level input current | $I_{IL}$(TXD) | VI=0 | -50 | | -10 | μA |
| The current of TXD when VCC=0V | $I_O$(off) | VCC=0V, TXD=5V | | | 1 | μA |
| Enter the upper limit of high voltage | $V_{IH}$ | | 2 | | VCC+0.3 | V |
| Enter the upper limit of low level | $V_{IL}$ | | -0.3 | | 0.8 | V |
| TXD port is suspended voltage | $TXD_O$ | | H | | | logic |

(If no other description is given, VCC=5V±5%, Temp=TMIN~TMAX, typical value in VCC=+5V, Temp = 25 )

## SPLIT Pin characteristics

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| SPLIT Output voltage | $V_O$ | -500uA<$I_o$<500uA | 0.3$V_{CC}$ | | 0.7$V_{CC}$ | V |
| Leakage current | $I_{O(stb)}$ | STB=2V, -12V<$V_O$<12V | -5 | | 5 | μA |

(If no other description is given, VCC=5V±5%, Temp=TMIN~TMAX, typical value is VCC=+5V, Temp = 25 )

## supply current

| Parameter | Symbol | Test condition | Minimum | Typical case | Maximum | Unit |
|---|---|---|---|---|---|---|
| Standby power consumption | $I_{CC}$ | STB=VCC, $V_I$=VCC | | 5 | 12 | μA |

| | | | | | | |
|---|---|---|---|---|---|---|
| Visible power consumption | | $V_I$=0V, STB=0V, LOAD=60Ω | | 38 | 70 | mA |
| Hidden power consumption | | $V_I$=VCC, STB=0V, NO LOAD | | 3.6 | 10 | mA |

(If no other description is given, VCC=5V±5%, Temp=TMIN~TMAX, typical value is VCC=+5V, Temp = 25 )

## Function table

Table 1 CAN transceiver truth table

| $V_{CC}$ | TXD(1) | STB(1) | CANH(1) | CANL(1) | BUS STATE | RXD(1) |
|---|---|---|---|---|---|---|
| 4.5V~5.5V | L | L | H | L | Dominance | L |
| 4.5V~5.5V | H (or floating) | X | $0.5V_{CC}$ | $0.5V_{CC}$ | Covert gender | H |
| 4.5V~5.5V | X | H (or floating) | $0.5V_{CC}$ | $0.5V_{CC}$ | Covert gender | H |
| 0<$V_{CC}$<4.5V | X | X | 0V<$V_{CANH}$<$V_{CC}$ | 0V<$V_{CANL}$<$V_{CC}$ | Covert gender | X |

(1) H= high level; L= low level; X= indifferent

Table 2 Driver Function Table

| INPUTS | | OUTPUTS | | Bus State |
|---|---|---|---|---|
| TXD(1) | STB(1) | CANH(1) | CAL(1) | |
| L | L | H | L | Dominate (dominant) |
| H (or floating) | X | Z | Z | Recessive (latent) |
| X | H (or floating) | Z | Z | Recessive (latent) |

(1) H= high level; L= low level; Z= high resistance; X= not concerned

Table 3 Receiver function table

| $V_{ID}$=CANH-CANL | RXD(1) | Bus State(1) |
|---|---|---|
| $V_{ID}$≥0.9V | L | Dominate (dominant) |
| 0.5< $V_{ID}$<0.9V | ? | ? |
| $V_{ID}$≤0.5V | H | Recessive (latent) |
| Open | H | Recessive (latent) |

(1) H= high level; L= low level;? = uncertain

## test circuit

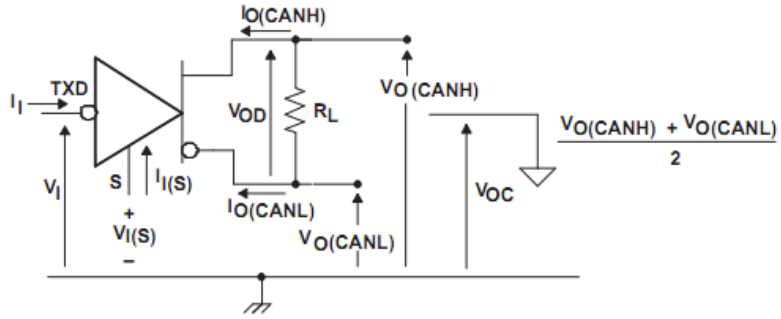



Figure 1 Definition of driver voltage and current test

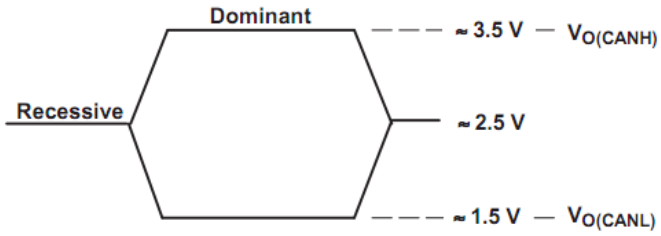



Figure 2 Bus logic voltage definition

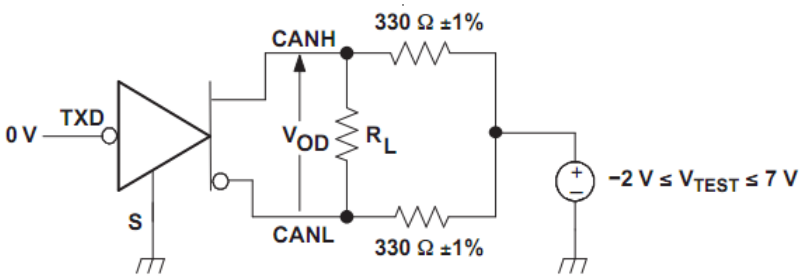



Figure 3 Driver VOD test circuit

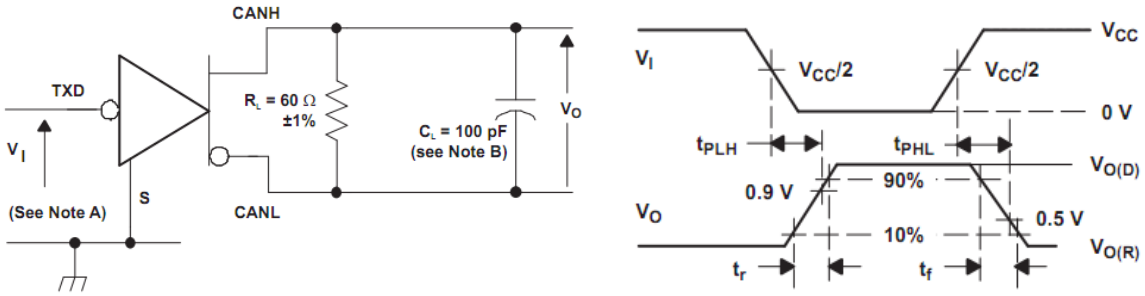



Figure 4 Driver test circuit and voltage waveform

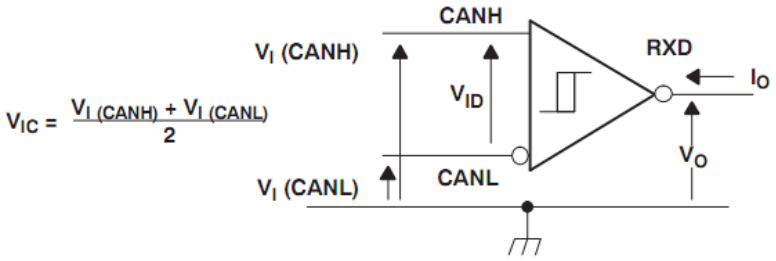
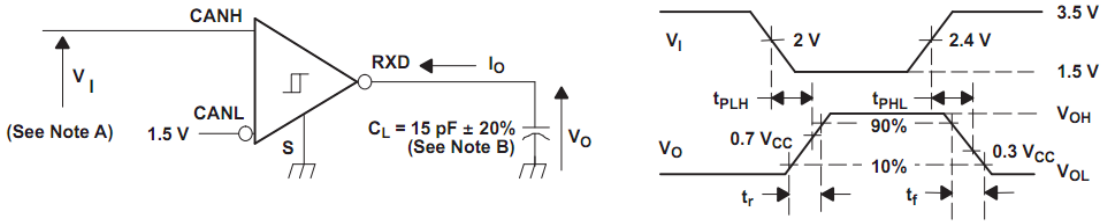



Figure 5 Receiver voltage and current definition




A. Characteristics of input pulse generator: PRR<=125KHz, 50% duty cycle, tr<6ns, tf<6 ns, Zo=50Ω

B, CL includes the instrument and fixed capacitor, and the error is within 20%.

Figure 6 Receiver test circuit and voltage waveform

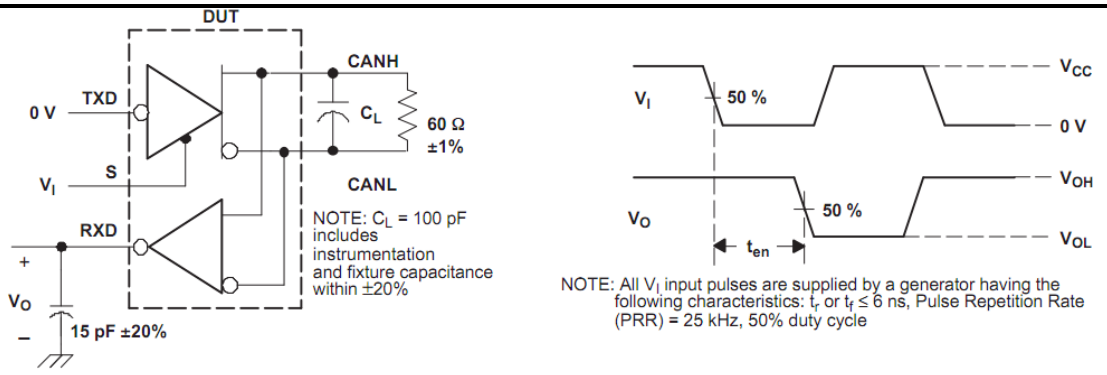
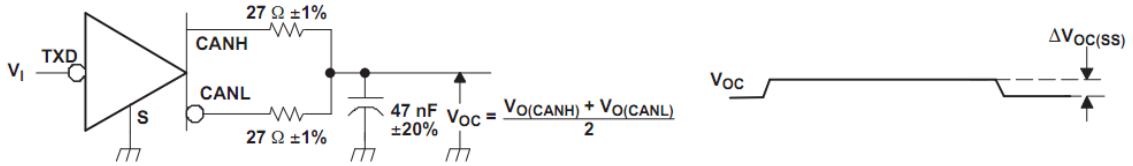



Figure 7 tEN test circuit and voltage waveform




Note: VI from 0 to VCC, input pulse generator characteristics: PRR<=125KHz, 50% duty cycle, tr<6ns, tf<6ns, Zo=50Ω

Figure 8 Common-mode output voltage test and waveform

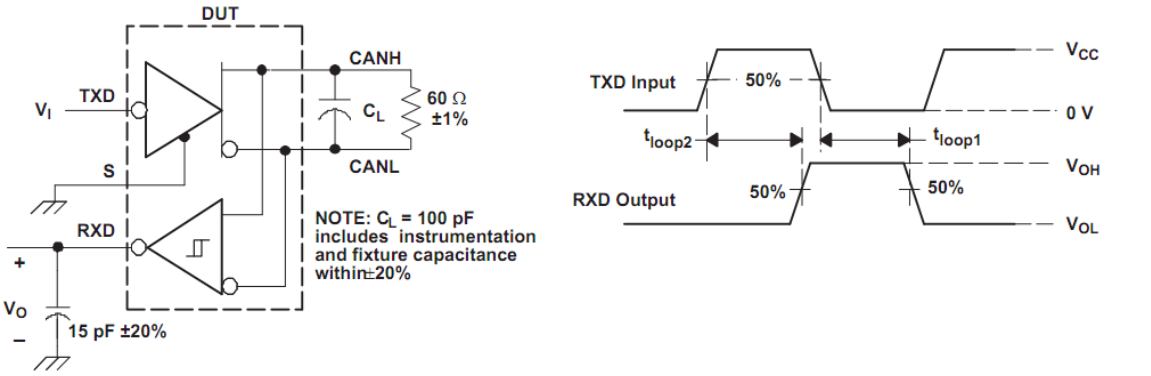



Figure 9 t (LOOP) test circuit and waveform

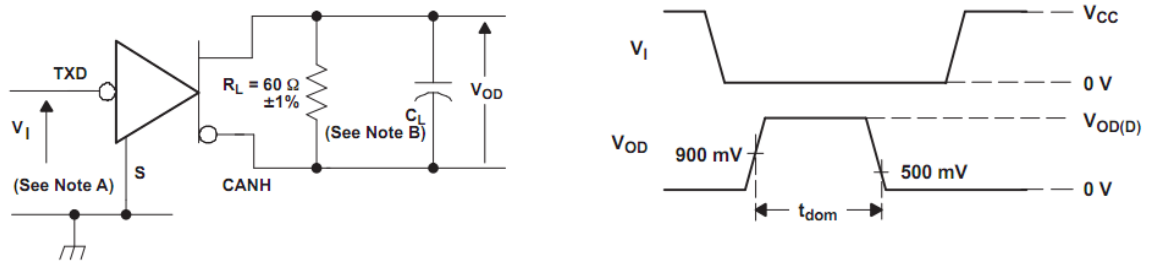



Figure 10 Explicit timeout test circuit and waveform

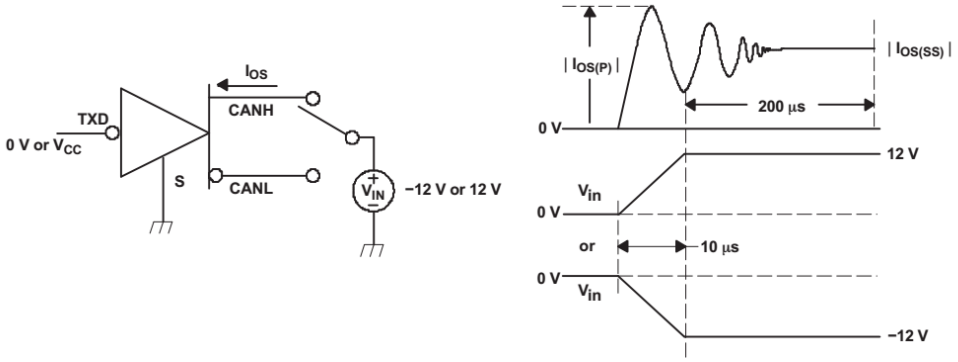



Figure 11 Circuit and waveform of short circuit current test for the driver

explain

## 1 resume

SIT1040Q is an interface chip applied between CAN protocol controller and physical bus, which can be used in truck, bus, car, industrial control and other fields. The rate can reach 1Mbps. It has the ability to transmit differential signal between bus and CAN protocol controller, and is fully compatible with "ISO 11898" standard.

## 2 short-circuit protection

The drive level of SIT1040Q has a current limiting protection function to prevent the drive circuit from short-circuiting to the positive and negative power supply voltage. When a short circuit occurs, the power consumption will increase. The short circuit protection function can protect the drive level from damage.

## 3 Failure safety

The TXD pin provides a pull-up path to VCC to ensure that the bus is in an implicit state when the TXD is not connected to power.

The STB pin provides a pull-up path to VCC to ensure that the transceiver is in standby mode when the STB is not powered.

When the VCC power is down, the TXD, STB and RXD pins will become floating to prevent reverse power supply through these pins.

## 4 Over temperature protection

SIT1040Q It has overtemperature protection function. After the overtemperature protection is triggered, the current of the driver level will be reduced, because the driver tube is the main energy consuming component, and the current reduction can reduce the power consumption and thus reduce the chip temperature. At the same time, other parts of the chip still maintain normal operation.

## 5 Visible timeout function

If the TXD pin is forced to a permanent low level due to hardware and/or software application failure, the built-in TXD explicit timeout timer circuit prevents the bus line from being driven into a permanent explicit state (blocking all network communications). The timer is triggered by a falling edge on the TXD pin.

If the low level on pin TXD persists for longer than the internal timer value (tdom), the transmitter is disabled and the drive bus enters a silent state. The timer is reset by a rising edge on pin TXD.

## 6 control model

The control pin STB allows for two operating modes:

High speed mode or standby mode.

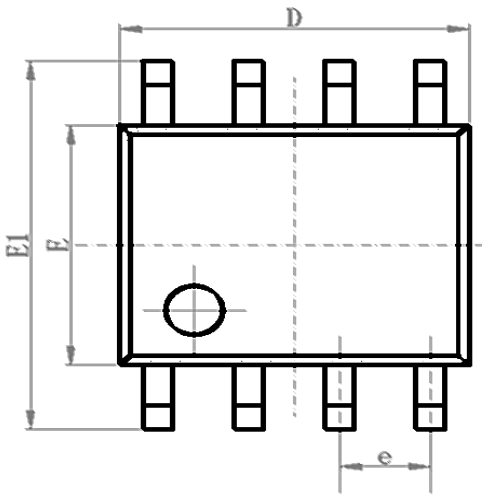
The high-speed mode is the normal operating mode, selected by grounding pin STB. The transceiver can send and receive data via CANH and CANL buses. The differential receiver converts the analog data on the bus into digital data and outputs it to pin RXD through a multiplexer (MUX).

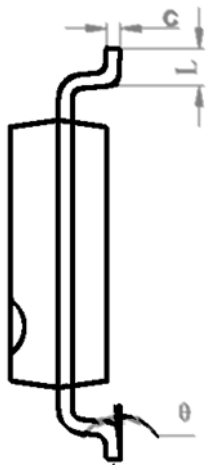
If the pin STB is at a high level or not connected, it operates in standby mode. In standby mode, the transmitter and receiver are turned off, and the bus lines are monitored by a low-power differential comparator. A high level on the pin STB activates this low-power receiver and wake-up filter. Once the low-power differential comparator detects a dominant bus level exceeding tBUS, the pin RXD will turn to a low level.

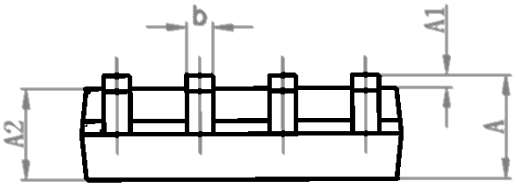
## SOP8, external dimensions

Package size

| Symbol | Least value /mm | Representative value /mm | Crest value /mm |
|---|---|---|---|
| A | 1.50 | 1.60 | 1.70 |
| A1 | 0.1 | 0.15 | 0.2 |
| A2 | 1.35 | 1.45 | 1.55 |
| b | 0.355 | 0.400 | 0.455 |
| D | 4.800 | 4.900 | 5.00 |
| E | 3.780 | 3.880 | 3.980 |
| E1 | 5.800 | 6.000 | 6.200 |
| e | | 1.270BSC | |
| L | 0.40 | 0.60 | 0.80 |
| c | 0.153 | 0.203 | 0.253 |
| θ | -2° | -4° | -6° |



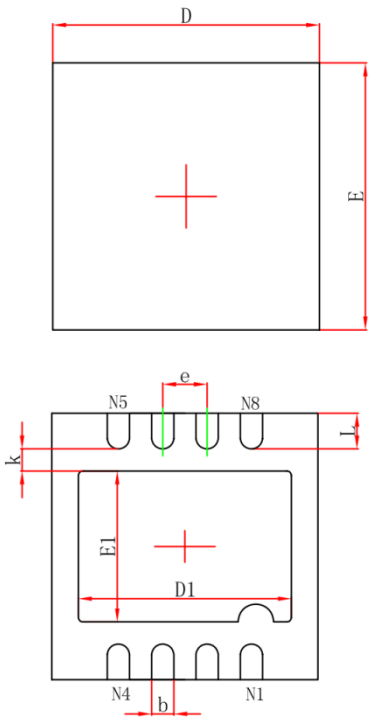



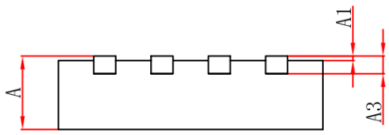



## HVSON8 / DFN3*3-8 shape

Package size

| Symbol | Least value /mm | Representative value / mm | Crest value /mm |
|---|---|---|---|
| A | 0.700 | | 0.900 |
| A1 | 0.000 | 0.02 | 0.050 |
| A3 | 0.203 REF | | |
| D | 2.900 | 3.000 | 3.100 |
| E | 2.900 | 3.000 | 3.100 |
| D1 | 1.400 | 1.5 | 1.600 |
| E1 | 2.200 | 2.3 | 2.400 |
| k | 0.275 REF | | |
| b | 0.2 | 0.25 | 0.33 |
| e | 0.650 TYP | | |
| L | 0.250 | | 0.575 |




## Order information

| Order code | Temperature | Package |
|---|---|---|
| SIT1040QT | -40℃~125℃ | SOP8 |
| SIT1040QTK | -40℃~125℃ | HVSON8 / DFN3*3-8, small shape, no pins |

SOP8 tape packaging is 2500 per disc, HVSON8 / DFN3*3-8, small form factor, and pinless packaging is 5000 per disc.