

Pulse width modulation circuit

summary

SG3524 is a pulse width modulation circuit used for switching power supply. It contains a reference voltage source, error amplifier, oscillator, pulse width modulation, pulse width control trigger, dual-way alternating output, current limiting circuit and turn-off circuit.

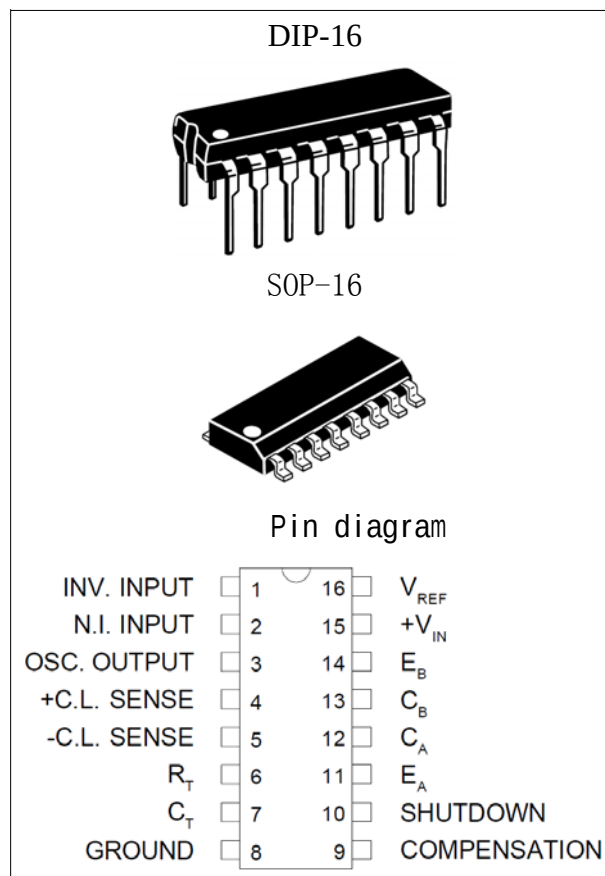
The circuit can be used for any polarity switch power supply control, transformer coupled DC-DC switch power supply, transformer boosting and polarity conversion, and other power supply applications.

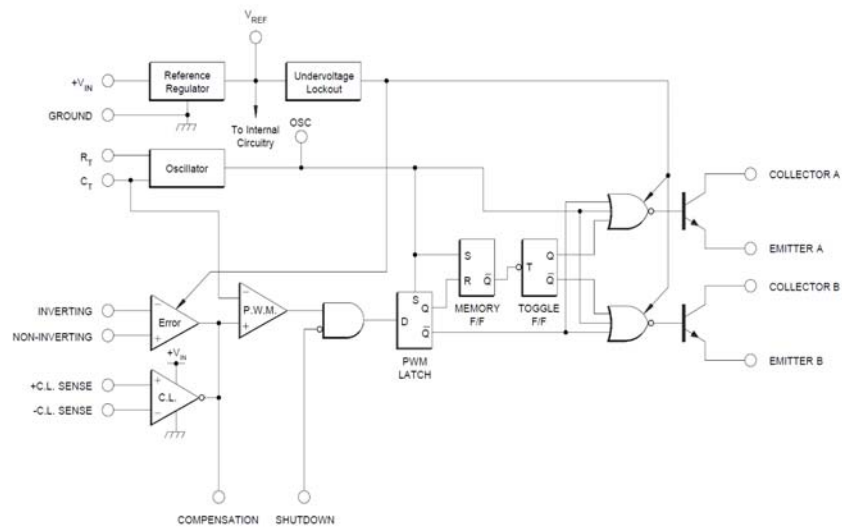
SG3524 Operating temperature is 0 to +70 .

main features

- It has a 5V reference voltage source.
- Oscillation frequency range of 100Hz to 300KHz.
- Good external synchronization capabilities.
- It has two 50mA outputs.
- Contains a current limiting circuit.
- Complete PWM control circuit.
- Single end or push-pull output.
- The total current consumption of the power supply is less than 10mA.

Internal function block diagram





Extreme parameters (absolute maximum rating, if no other provisions, Tamb = 25)

Name (symbol)	Price	Unit
Input voltage (Vin)	42	V
Collector voltage	40	V
Logic input voltage	-0.3~5.5	V
Current limiting foot difference input (Vsense)	-0.3~0.3	V
Output current per channel	100	mA
Baseline voltage load	40	mA
Charging current at the oscillation end	5	mA
Junction temperature	150	℃
Operating ambient temperature	0~70	℃

Recommend working conditions

Name (symbol)	Price	Unit
Input voltage (Vin)	8~40	V
Collector voltage	0~40	V
The common mode input voltage of the error amplifier	1.8~3.4	V
Current limiting foot difference input (Vsense)	-0.3~0.3	V
Output current per channel	0~50	mA
Baseline voltage load	0~20	mA
Charging current at the oscillation end	0.03~2	mA
Oscillation frequency	0.1~300	KHz
Oscillating resistance (Rt)	1.8~100	K Ω
Oscillating capacitor (Ct)	1~1000	nF
Junction temperature	150	℃
Operating ambient temperature	0~70	℃

Electrical parameters (Vin=20V, TA=25 unless otherwise specified)

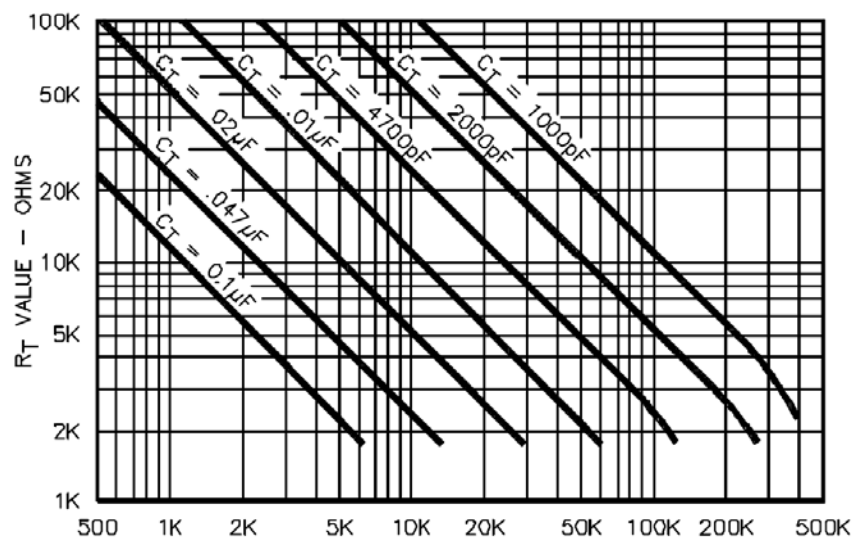
Symbol	Parameter	Condition	SG3524			Unit
			MIN.	TYP.	MAX.	
Reference voltage section Vref (IL = 0mA when not specified)						
Vref	Output voltage		4.8	5.0	5.2	V
Line Reg	Voltage linearity	Vin=8V~40V			30	mV
Load Reg	Load linearity	IL = 0 to 20mA			50	mV
Short current	Base short-circuit current	VREF = 0V	25		150	mA
Oscillation part Oscillator (FOSC = 40KHz, RT = 2.9KW, CT =0.01uF when no description)						
Fosc	Oscillation frequency		36		44	KHz
	Frequency voltage drift	VIN = 8V to 40V			1	%
MaxFosc	Maximum oscillation frequency	RT = 2K, CT = 1nF	200	400		KHz
	Oscillating waveform peak		3		3.9	V
	Oscillating waveform valley		0.6		1.2	V
Pulse Width	Oscillation pulse width		0.3		1.5	us
Error amplifier part EA (Vcm=2.5V when no description is given)						
Vio	Input offset voltage				10	mV
Ib	Input bias current				10	uA
Iio	Input offset current				2	uA
Av	DC open-loop gain		60			dB
Vol	Output low level	VPIN 1 – VPIN 2 > 150mV		0.2	0.5	V
Voh	Output high level	VPIN 2 – VPIN 1 > 150mV	3.8	4.2		V
CMR	Input common mode suppression	VCM = 1.8V to 3.4V	70			dB
PWM comparator section						
Min Duty	Minimum duty cycle	VCOMP = 0.5V			0	%
Max Duty	Maximum duty cycle	VCOMP = 3.6V	45	49		%
Current limiting circuit section Current Limit Amplifier (VCM = 0V)						
Vsense	Enter the threshold voltage		180		220	mV
Ib	Input bias current				200	uA
The circuit is turned off at Shutdown						
Vth	Turn off the threshold voltage		0.5	0.8	1.2	V
Output section (each output)						
Cleak	Collector leakage current	VCE = 40V			50	uA
Vcsat	Collector voltage	IC = 50mA			2	V

	drop					
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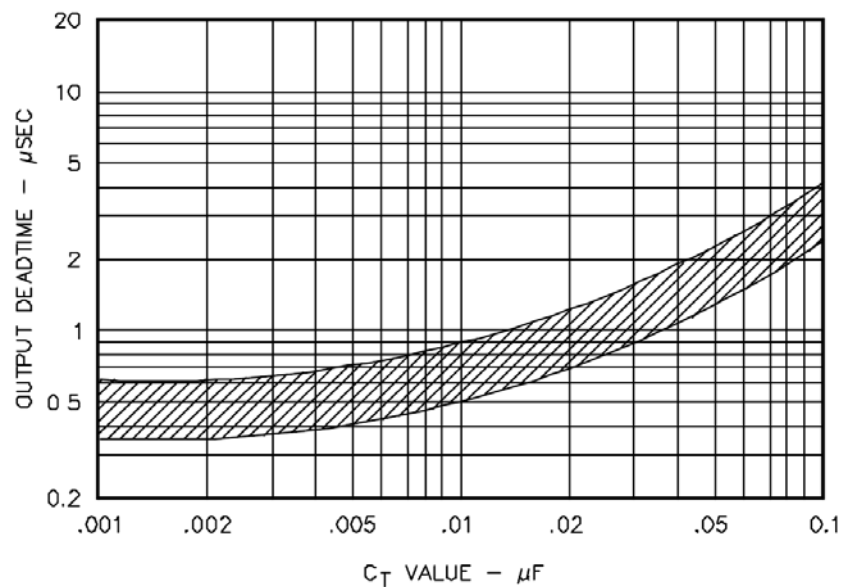
Symbol	Parameter	Condition	SG3524			Unit
			MIN.	TYP.	MAX.	
V_e	Output voltage of the emitter	$I_E = 50\text{mA}$	17			V
Rise time	Cathode output rise time	$R_C = 2\text{K}$			0.4	μs
Fall time	Collector output fall time	$R_C = 2\text{K}$			0.2	μs
The circuit as a whole						
I_{cc}	Static operating current	$V_{IN} = 40\text{V}$			10	mA

Applications and annotations

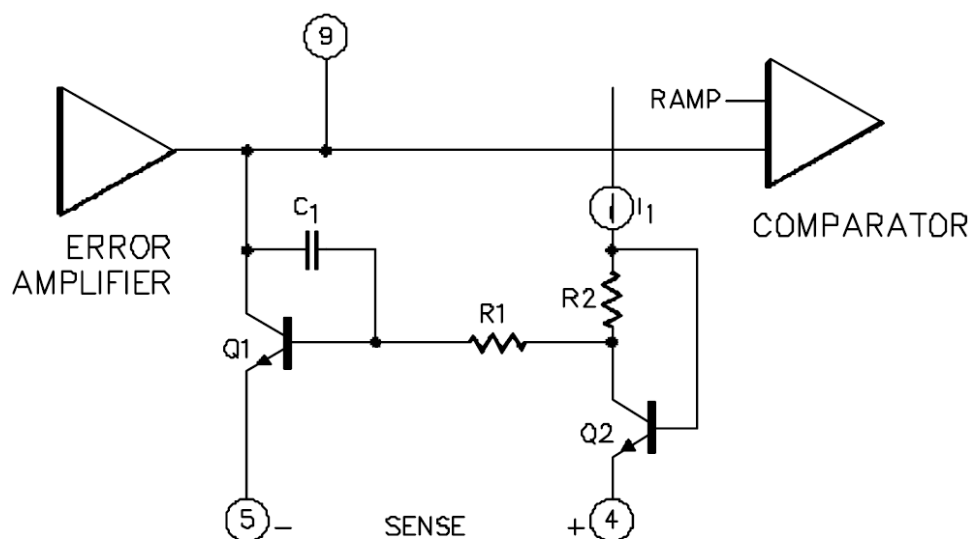
1. Table 1 (Relationship between oscillation frequency and R_t , C_t)



2. Table 2 (Relationship between dead time and Ct)

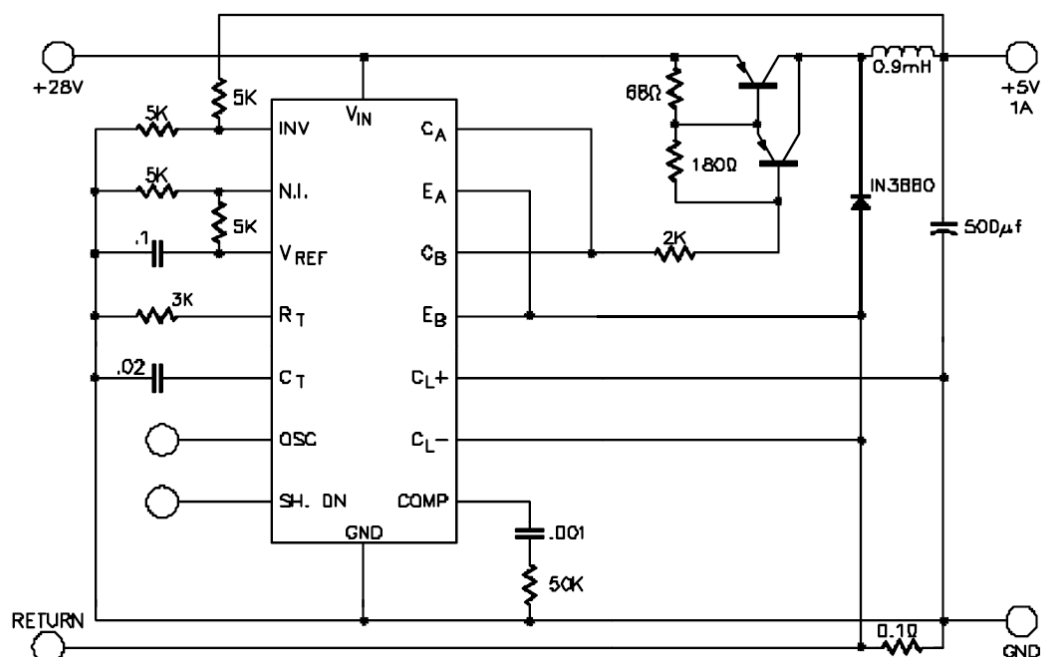


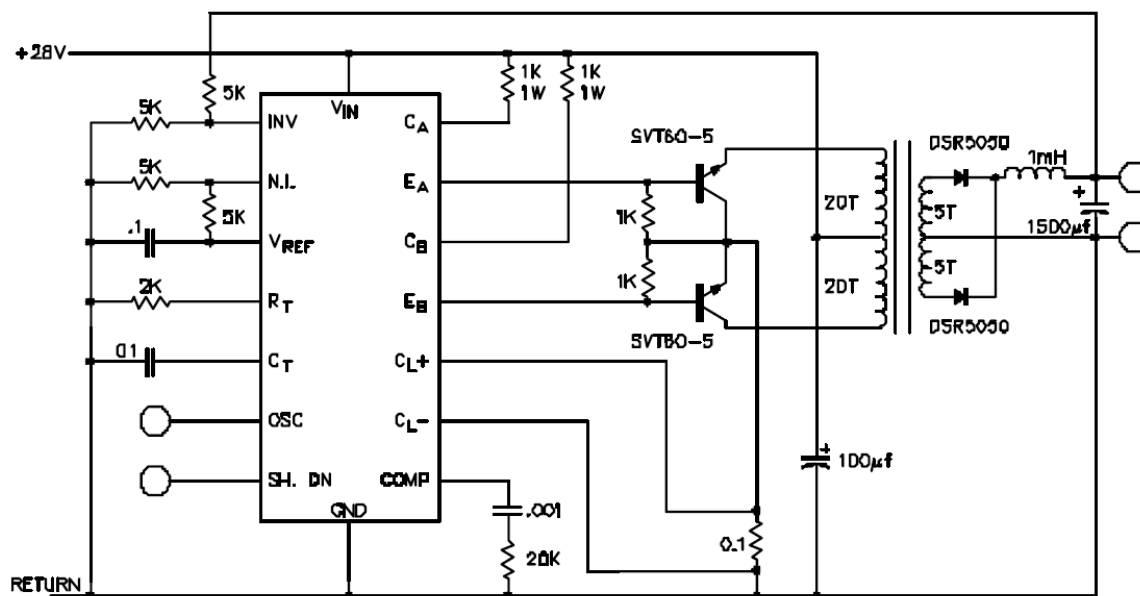
3. Internal current limiting circuit wiring diagram



$$\text{C.L. Threshold} = V_{BE}(Q1) + I_1 \cdot R_2 - V_{BE}(Q2) = I_1 \cdot R_2 \sim 200 \text{ mV}$$

4. Single-ended output application (terminal output control can reach 0~90% duty cycle)





package

