1. DESCRIPTION

The XD3403 is a low cost, quad operational amplifier with true differential inputs.

the XD3403 has several distinct

advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents

The common modeinput range includes the negative supply,

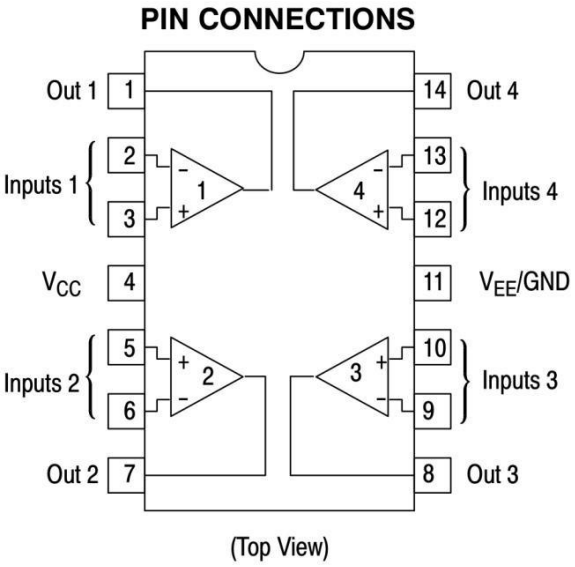
thereby eliminating the necessity for external biasingcomponents in many applications.

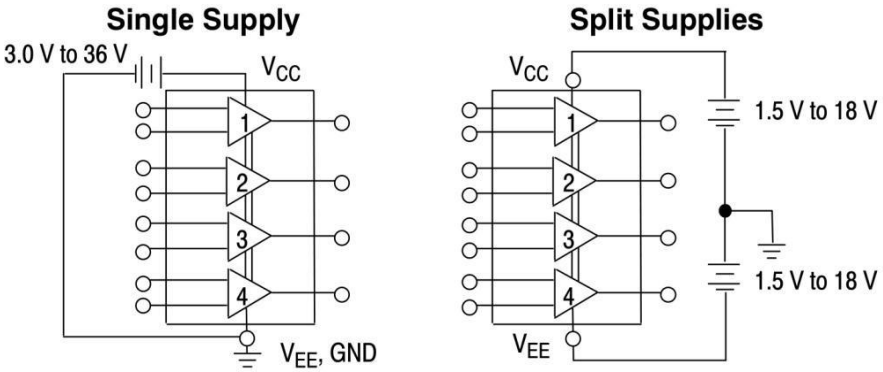
The output voltage range also includes the negative powersupply voltage.

2. FEATURES

- Unity gain band width-3.0 MHz
- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated

3. PIN CONNECTIONS





4. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	 36 ±18	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range (Notes 1 and 2)	V_{ICR}	±18	Vdc
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Ambient Temperature Range XD3403	T_A	 0 to +70	°C
Junction Temperature	T_J	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Split power supplies.
2. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

5. ELECTRICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V for XD3403)

Characteristic	Symbol	XD3403			Unit
		Min	Typ	Max	
Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 3)	V_{IO}	– –	2.0 –	10 12	mV
Input Offset Current T_A = T_{high} to T_{low}	I_{IO}	– –	30 –	50 200	nA
Large Signal Open Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ $T_A = T_{high}$ to T_{low}	A_{VOL}	 20 15	 200 –	 – –	V/mV
Input Bias Current T_A = T_{high} to T_{low}	I_{IB}	– –	−200 –	−500 −800	nA
Output Impedance f = 20 Hz	z_o	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, T_A = T_{high} to T_{low}	V_O	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	V
Input Common Mode Voltage Range	V_{ICR}	+13 V −V_{EE}	+13 V −V_{EE}	–	V
Common Mode Rejection $R_S \leq$ 10 kΩ	CMR	70	90	–	dB
Power Supply Current (V_O = 0) R_L = ∞	I_{CC}, I_{EE}	–	2.8	7.0	mA
Individual Output Short−Circuit Current (Note 4)	I_{SC}	±10	±20	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR−	–	30	150	μV/V
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	μV/°C
Power Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 20 V(p−p), THD = 5%	BWp	–	9.0	–	kHz
Small−Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	–	1.0	–	MHz
Slew Rate A_V = 1, V_i = −10 V to +10 V	SR	–	0.6	–	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	os	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, V_O = 200 pF	ϕm	–	60	–	°
Crossover Distortion (V_{in} = 30 mVpp, V_{out} = 2.0 Vpp, f = 10 kHz)	–	–	1.0	–	%

Characteristic	Symbol	XD3403			Unit
		Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	nA
Input Bias Current	I_{IB}	–	−200	−500	nA
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	10	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	μV/V
Output Voltage Range (Note 5) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 ≤ V_{CC} ≤ 30 V	V_{OR}	 3.3 V_{CC}−2.0	 3.5 V_{CC}−1.7	 – –	V_{pp}
Power Supply Current	I_{CC}	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	CS	–	−120	–	dB

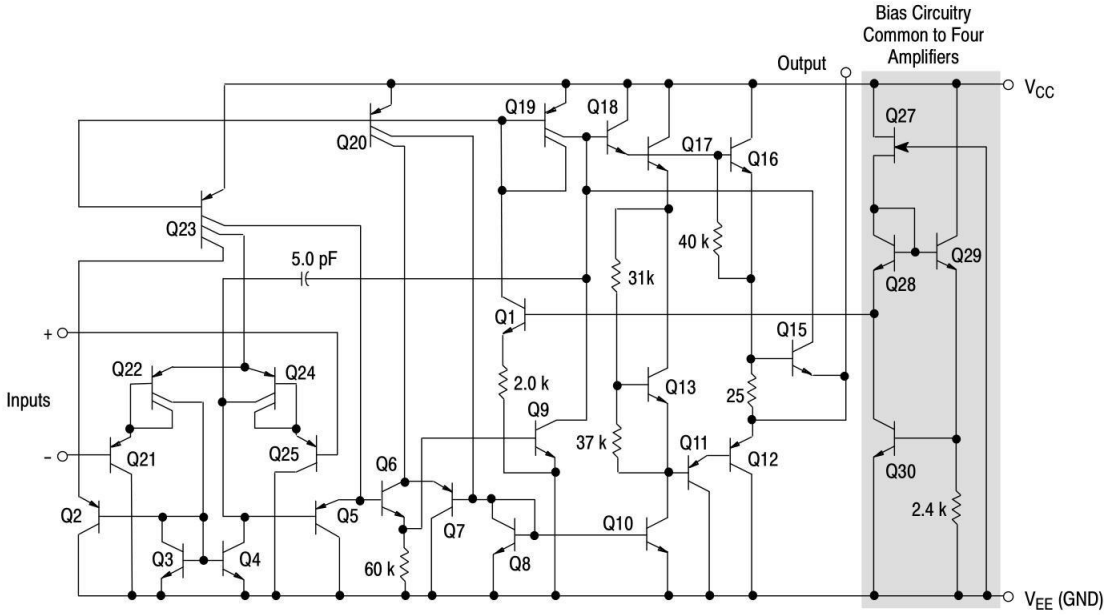


Figure 1. Representative Schematic Diagram
(1/4 of Circuit Shown)

6. CIRCUIT DESCRIPTION

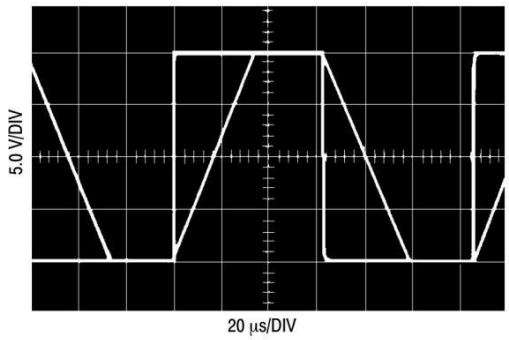


Figure 2. Inverter Pulse Response

The XD3403 is made using four internally compensated, two − stage operational amplifiers. The first stage of each consists of differential input device Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and Transconductance reduction functions. By reducing the Transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The Transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single − ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient, thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

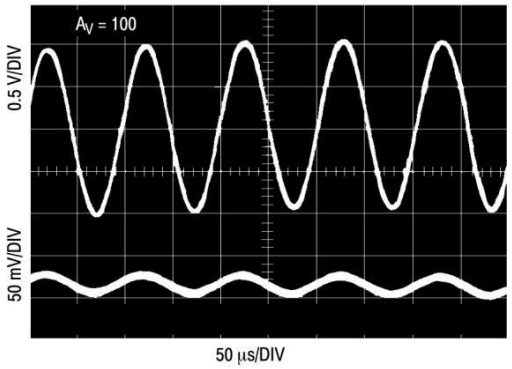


Figure 3. Sine Wave Response

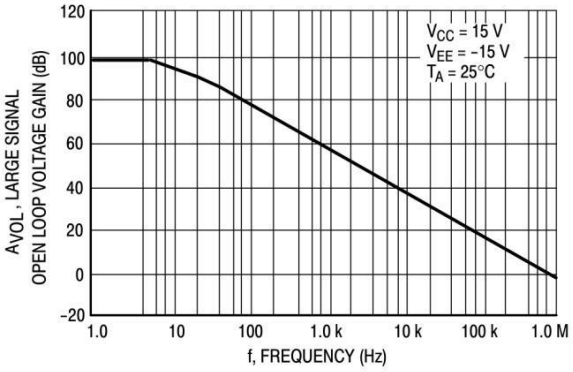


Figure 4. Open Loop Frequency Response

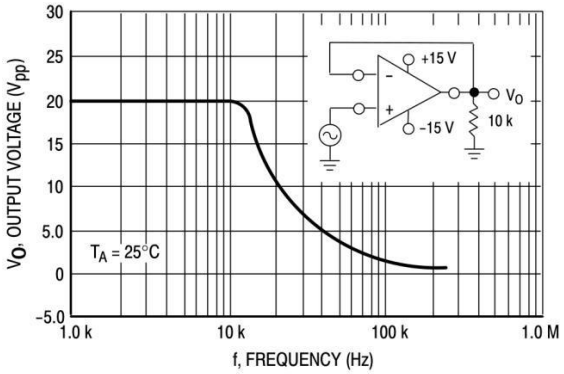


Figure 5. Power Bandwidth

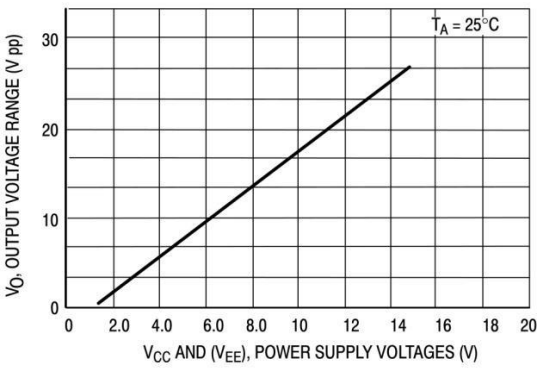


Figure 6. Output Swing versus Supply Voltage

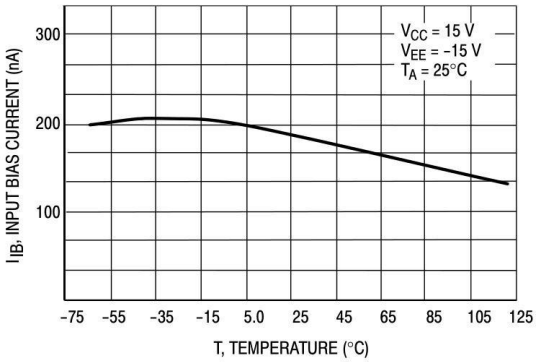


Figure 7. Input Bias Current versus Temperature

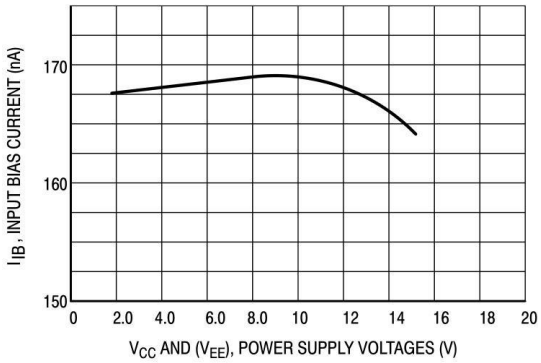


Figure 8. Input Bias Current versus Supply Voltage

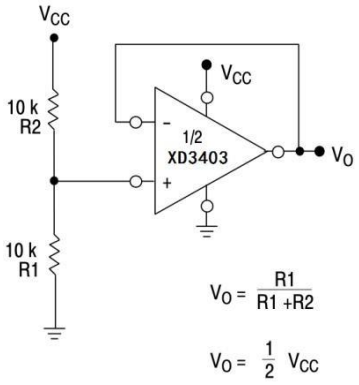


Figure 9. Voltage Reference

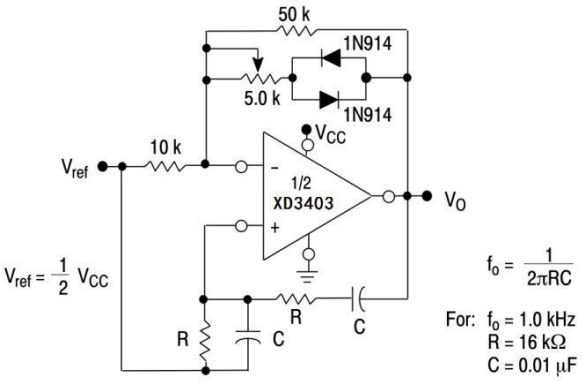


Figure 10. Wien Bridge Oscillator

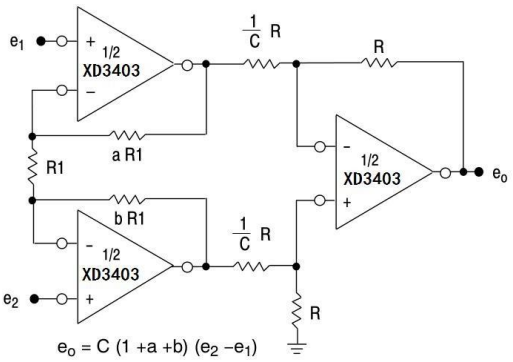


Figure 11. High Impedance Differential Amplifier

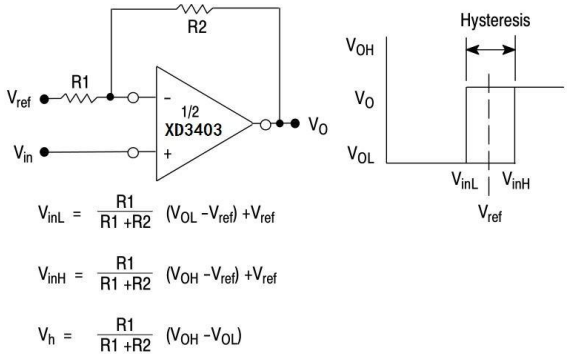


Figure 12. Comparator with Hysteresis

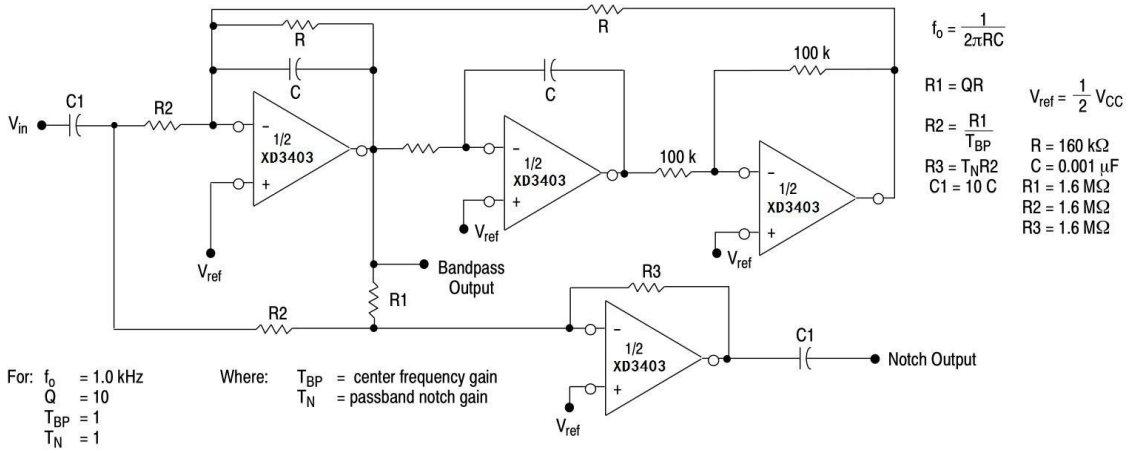


Figure 13. Bi–Quad Filter

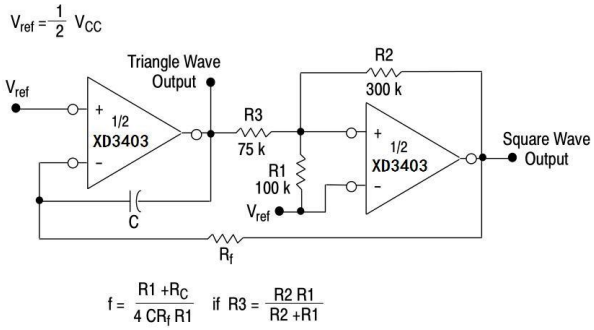


Figure 14. Function Generator

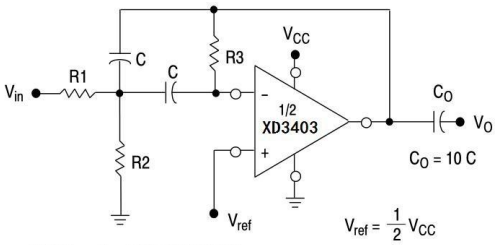


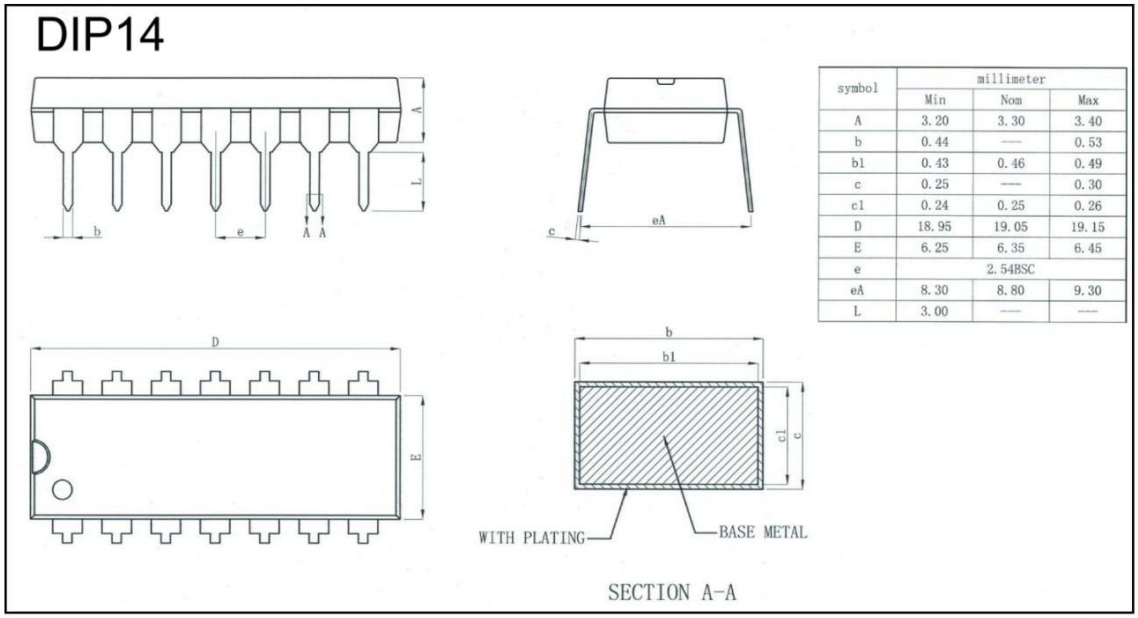
Figure 15. Multiple Feedback Bandpass Filter

7. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (℃)	MSL	Transport Media	Package Quantity
XD3403	XD3403	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

8. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	——	0.53
b1	0.43	0.46	0.49
c	0.25	——	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	——	——